VDA-Place: Voltage-Drop-Aware Standard Cell Placement

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ABSTRACT

Voltage drop is becoming increasingly significant as integrated circuit (IC) fabrication processes move beyond 45nm, affecting both timing and reliability. We propose an IR-Drop based detailed standard cell placer that can achieve significant optimization of up to 6% for the timing of the critical path of a design. Our placer works incrementally to existing placers and is, thus, easier to integrate into existing industrial design flows.

KEYWORDS

Algorithms, physical design, placement, voltage drop, IR-drop.

1 INTRODUCTION

As the fabrication processes of integrated circuits (IC) progress beyond 45nm, the voltage drop on the power supply network becomes a very important issue, affecting both the timing and the reliability of the IC. Several academic and industrial solutions have been proposed for accurately estimating the voltage drop and for optimally designing [1], [2], [3], [4], [5], [6], [7], [8], [9], [10] the power supply network of an IC. The target of all estimation approaches is to identify which areas of the design suffer from high voltage drop that adversely impacts the timing of the gates in that area, and, consequently, the performance of the entire circuit if the aforementioned gates happen to be on the critical path of the design. In the case where the voltage drop of the area encompassing part of the critical path of a design appears to be outside the required voltage drop limit the only course of action can be taken in present industrial design methodologies is to redesign the power grid and recalculate the voltage drop until it falls within the prescribed limits. However, this can happen late in the design cycle and induce a significant delay in the design cycle of the IC. Furthermore, even if the critical path is within the voltage drop bounds, negative slack can be present, which can be fixed either by upsizing the gates of the critical path or by restructuring the logic and the gates that implement it. Both of the above actions late in the design process may cause unnecessary perturbations and impede the convergence of the design.

The approach presented in this paper is a first attempt at altering the prevalent design methodology by addressing the timing issues that arise when the critical path of a design is in a high voltage drop area either within or outside the prescribed limit. The main idea is to alter the placement of the critical path gates in such a way that they are moved to low voltage drop areas, and, therefore, suffer less performance reduction due to voltage drop. In the case where negative slack persists at the end of the design process, moving the critical path cells to a low voltage drop area is equivalent to speeding up the circuit under worst-case conditions, removing thus negative slack and providing another design knob that can be tweaked to optimize the design without the significant overhead that is introduced by extensive circuit or logic changes

In the remainder of this paper, Section 2 introduces our key ideas and articulates our placement algorithm, Section 3 describes the methodology used for the IR-Drop based placement and Section 4 summarizes our results. Conclusions are presented in Section 5 and extensions and improvements are discussed.

2 VOLTAGE DROP AWARE PLACEMENT ALGORITHM

The standard placement methodology consists of four phases: initial placement, global placement, detailed placement and legalization as shown in Figure 1. The proposed methodology intervenes at the detailed placement level and directs the critical path cells towards low voltage drop areas, while taking into account the timing overhead induced by potentially longer interconnect lines between the critical path cells. For the purposes of this approach it is assumed that the overall voltage drop pattern of the circuit is not altered significantly, if at all, by the alternate placement of the critical path cells. This is a quite moderate assumption as the critical path cells are usually less than 20 in a design typically exceeding 10K cells.

The available placement area for each circuit is pessimistically computed by the following expression:

$$placement\_area = n\% \times total\_cell\_area \quad (1)$$

Where *n* is a measure of the white space available after the placement process, which includes an overhead to be used for ECOs late in the design process such as the ones that are the result of our approach.

For the purposes of the proposed methodology the placement area is assumed to be rectangular with no obstructions, which is a safe assumption to make for a standard cell placer (but not for a mixed-size placer). The inputs and outputs of the overall design are considered to be points and are placed in the periphery of the placement area, with their spacing defined by the parameters of the fabrication process. In order to obtain test structures for applying the voltage drop aware techniques, we have used our own placement platform to generate a number of test cases based on the ISCAS 89 and ITC 99 benchmark suites [11], [12].

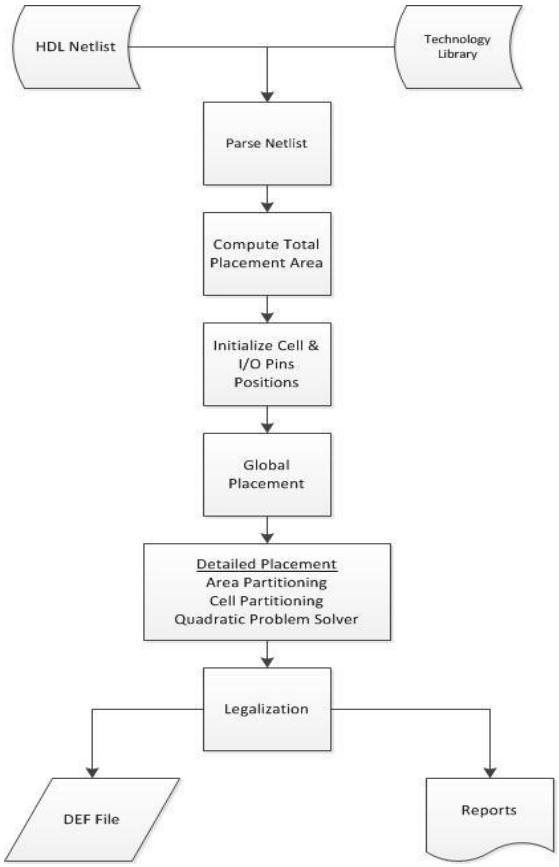

Figure 1. Placement flow

2.1 Initial Placement Conditions

The initial positioning of the input and output pins is random, based on the convention that inputs are positioned in the upper and left side and outputs are positioned in the right and lower side of the rectangular. These initial conditions are necessary as the global placement algorithm that has been used is based on the Gordian framework, and fixed placement

of the pins at the periphery of the chip area is a requirement.

2.2 Global Placement

A global partition that extends to the whole available area and contains all the cells of the design is defined. We model the optimal positioning of the cells by formulating a quadratic problem following the same steps as the Gordian algorithm [13]. Gordian performs global optimization and rectangle dissection. The algorithm uses global optimization at all steps trying to minimize a cost function that describes the formulated quadratic problem. The cost function is as follows:

$$cost=0.5\mathbf{x}^T\mathbf{Q}\mathbf{x}+d_x^T+0.5\mathbf{y}^T\mathbf{Q}\mathbf{y}+d_y^T\mathbf{y}+\mathbf{const} \quad (2)$$

Where x and y are the solution vectors, const is a constant that is derived from information about chip constraints such as fixed modules, Q is the Laplacian matrix and d_x and d_y are fixed pins vectors.
The solution of this problem provides the optimal position for each cell considering the interconnect wire-length. The possibility of cells overlapping forces the use of a legalization method [14] in order to obtain an initial solution.

2.3 Detailed Placement

This iterative phase consists of here steps: area partitioning, cell partitioning and quadratic problem solution. The iterations conclude when there are no sub-partitions left that meet the cell and area specifications we have set (sub-partition size and cell count). We kept the area partitioning method simple. The cut line is placed in the larger side of the rectangular and more specifically in the interval between the middle and the end of the side. The validation of the newly formed partition is based on a number of criteria with the most important being the following:

1. The new partition must contain a total number of cells bigger than a predefined number (in our case four), based on the analysis depth we want to achieve.
2. The height or width of the new partition, depending on the direction of the cut line, must be at least four times the length of its larger cell.
3. The new cut point must be sufficiently different from cut points chosen in previous iterations of the algorithm.
4. The cells contained in the new partition must cover an amount of area smaller than the area of the new partition.

By accumulating these criteria the number of test areas is reduced and therefore the overall execution speed of the algorithm is reduced without lowering the quality of the final solution.
For the cell partitioning the Kernighan-Lin partitioner [15], [16] is used in order to acquire the optimal way to spread the cells between two newly formed partitions. For connected cells that are moved in different partitions pseudo-pins are created at the periphery of the partition to balance their movement ability.
When the new partitions have been defined new quadratic problems can be formulated, specific for each partition, based in the steps of the Gordian algorithm.

2.4 Legalization

Following the solution of the quadratic problem of each sub-partition, the Abacus algorithm for legalization is applied in order to eliminate any cells overlapping. The pseudo-code for the Abacus legalization approach is presented in the following segment:

```
foreach cell I do
      best_cost ← ∞;
      foreach row r do
            Insert cell I into row r;
            placerow r (trial);
            determine cost c;
            if c < best_cost then
```

```
                best_cost=c;
                r_best=r;
            remove cell I from row r;
        end
        insert cell I to row r_best;
        placerow r_best (final);
end
```

3 IR-DROP BASED PLACEMENT

Voltage drop occurring during the operation of a circuit affects the overall timing. If the cells are not suitably supplied voltage, they cannot reach the desired level within the rise time that characterizes them. Based on that observation we present an extension to our algorithm for the re-placement of a pre-placed design based on the IR-drop analysis of the circuit.

The algorithm takes into account data of an IR-drop analysis that define the voltage drop in each cell, and creates a general voltage drop mapping for the design. Subsequently, it detects the most timing critical path of the design and checks which cells contained in this critical path can be exchanged with other cells in irrelevant parts of the design.

Our greedy approach is based in finding and exchanging the cell with the biggest voltage drop from the critical path, with the cell that is not contained in the aforementioned path and displays the lowest voltage drop. The total number of interchanges is not pre-defined. Our algorithm comes to a halt when there are no more advantageous exchanges left to be made.

In the final step of this approach the cell positions are legalized. The cell movement is kept to a minimum and to the direction that contains the largest free space.

Figure 2 presents a simple example of the proposed methodology by which the cells of a critical path could be moved based on our algorithm. The figure depicts a chip where the darker colored areas present higher voltage drop compared to the lighter colored areas, and a final placement for the critical path. By applying our algorithm, the critical path cells are moved to lighter areas trading off between a better timing for the overall design and an insubstantial increase in interconnect length.

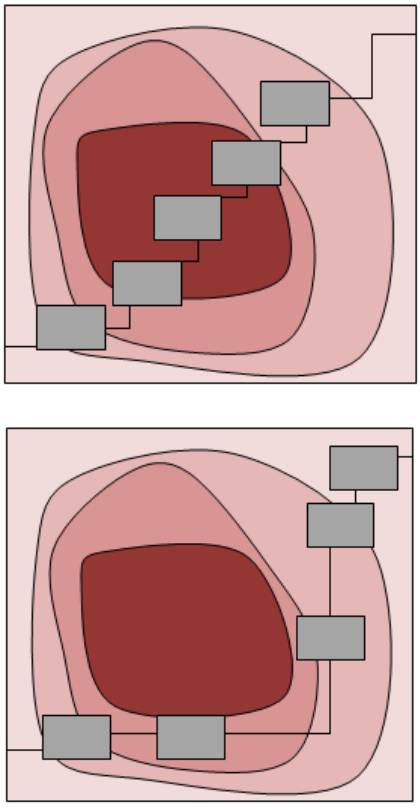

Figure 2. IR-Drop based placement of the critical path

The overall critical path delay can be computed as the sum of the delays of each cell that are a part of it. The new delay that characterizes a cell after its placement can be estimated by the following formula:

$$new\_cell\_delay = old\_cell\_delay \times (V_{dd\_old} - V_t)/(V_{dd\_new} - V_t) \quad (3)$$

Where V_{dd} is the threshold voltage and:

$$V_{dd} = V_{nom} - IR\text{-}Drop \quad (4)$$

The execution flow of our IR-Drop based placement algorithm can be seen in Figure 3.

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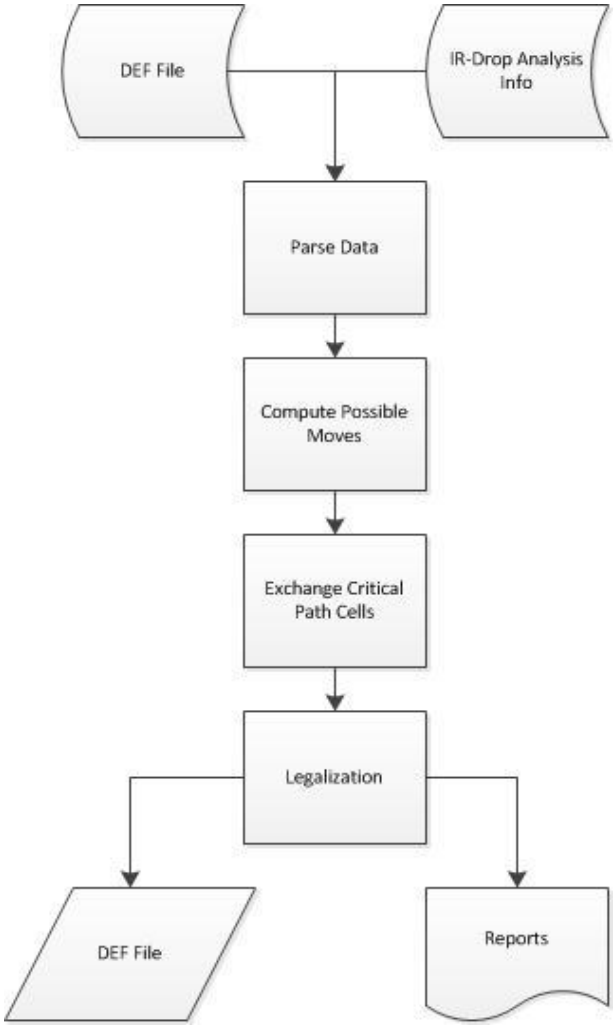

Figure 3. IR-Drop based placement flow

4 RESULTS

This section presents the results that were obtained from the application of our algorithm to the ISCAS'89 and ITC'99 benchmark circuits. The basic metric used was the overall optimization of the critical path's timing.
Figure 4 presents the results of our approach for the largest circuits of the above benchmark suites. Our voltage-drop-aware approach was pitted against the current voltage-drop-oblivious methodology used by all design teams in industry.

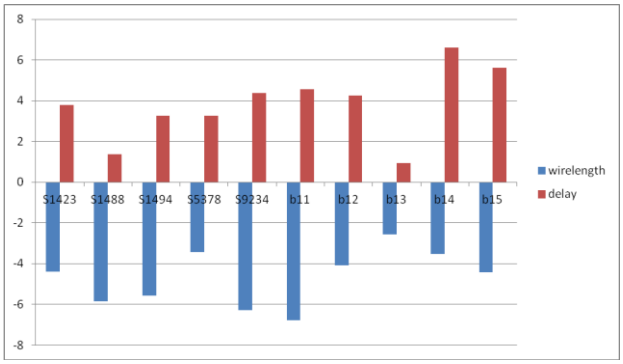

Figure 4. IR-drop based placement, ISCAS'89 and ITC'99 critical path timing and wire-length optimization percentages.

It becomes evident that our approach does produce significant timing improvements that offsets the small interconnect length increase. Since the current design methodology, as was previously stated, is voltage-drop oblivious, it can be expected that the same timing improvement will be present even at the most advanced, timing pressed designs. Given the fact that industrial designs strive to gain even a fraction of a percentage point in timing improvement, the average of 3.5% timing gain is extremely significant.

5 CONCLUSIONS AND FUTURE WORK

In this paper we developed a new quadratic placer for IR-Drop critical designs. Unlike other placers, it was simpler and our implementation included fewer than 10.000 lines of C code [17]. Our final conclusion, based on the results of the previous section, is that, under certain conditions, a greedy exchange between cells of the critical path and cells from other parts of a circuit based solely in their voltage drop can lead to significant improvement of the critical path's timing while deteriorating total wire-length at acceptable levels.
This approach could be extended to take into account multiple critical paths with varied significance for a design. In addition, the greedy selection algorithm could incorporate heuristic criteria based on the individual characteristics of each circuit.

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