LTE handset RF power consumption emulation

Deogratius Musiige* , Laulagnet Vincent*, François Anton †, Darka Mioc †
* Renesas Mobile Europe
Sluseholm 1, 2450 Copenhagen SV, Denmark
Email:{Deogratius.musiige, Vincent.Laulagnet}@renesasmobile.com
†National Space Institute, The Technical University of Denmark
Building 321, 2800 Kgs. Lyngby, Denmark
Email: { mioc, fa} @space.dtu.dk

***Abstract*—This paper presents a new methodology for the emulation of power consumption of the RF portion of a cell phone/ handset when transmitting a LTE signal. The inputs to the emulation are baseband-RF subsystem logical interface parameters such as bandwidth, carrier frequency, TX power. The dissipated power is measured at discrete values of the variables, and the emulated power is obtained by a $4 \times 5 \times 1$ neural network applying Pseudo-Gauss-Newton optimization algorithm. The methodology has been validated to have an accuracy of 94.3% though this is constrained by the measurement uncertainty of 11%. A FTP upload scenario in motion is used to illustrate the emulation methodology. A homotopy mapping method described in this paper is able to model the power consumption of the RF subsystem of a handset operating at a carrier frequency of 1.95 GHz with a 10 MHz signal bandwidth, from measured data at 1.4 and 20 MHz signal bandwidths with an error of only 1%.**

***Index Terms*—Radio frequency, High Power Amplifier, Baseband, LTE, Power, Emulation, Homotopy, Interval analysis, Tx power, Register-Transfer Level.**

I. Introduction

The rapidly growing wireless telecommunication technology demands high data rates at low costs and low power consumption. Sophisticated modulation and access schemes such as OFDM in LTE [2] have been introduced to increase capacity and meet the high data rate demands. In a handset, the low cost and low power consumption criteria are heavily influenced by both the baseband (BB) and radio-frequency (RF) components [3] of the modem. A power consumption analysis of a smartphone [4] showed that the modem consumes 80.6% and 59% of the total smartphone power (excluding the blacklight) for a GSM phone call and General Packet Radio Service (GPRS) emailing, respectively.

It is of interest to be able to predict the average power consumption of the handset during the design process as it relates to the different components. A formal method to achieving this prediction is referred to as *emulation*, which is in this work the analysis of dissipated power with a goal of optimization prior to mass production of handsets. To emulate the power consumption of the RF portion of the handset, the input parameters to the emulation are combinations of carrier frequency, transmitted power, signal bandwidth, and modulation scheme, taken from the logical interface between the BB and RF sub-systems during realistic operation. The output of the emulation is the average consumed power in a 1-ms sub-frame in case of LTE. The emulation method needs to reflect precisely the system that will be implemented [5]. Emulation is not to be confused with simulation, which typically refers to modeling towards an optimal solution given a set of predefined metrics [5].

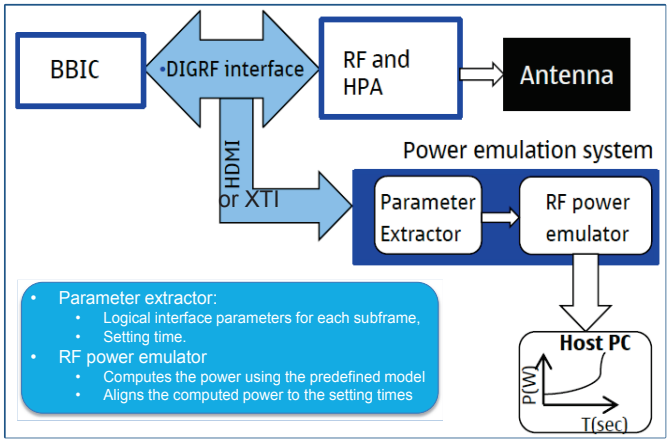


Fig. 1: The RF power emulation system, monitors the stream of the logical commands over the DIGRF interface, extracts the RF subsystem power dependent parameters in the "Parameter extractor" module and computes the emulated power in the "RF power emulator" module.

Extensive work has been published on the estimation of power consumption at various levels of abstraction [6]–[9]. Figure 2 shows the levels of abstraction during the design of *SoC (System-on-Chip)* systems. We can observe that the amount of information increases by an order of magnitude as the design maneuvers from system level to transistor level [10]. Consequently, the accuracy of power consumption estimation also increases as more knowledge is gained when the design transverses from the system level to the transistor level.

Approaches for power estimation at different levels of abstraction have been commercialized into power estimating tools [12]–[17]. The applicability of the PowerTheater [15], SpyGlass [13] and Cadance power estimation [12] tools were analyzed in a feasibility study conducted by Nokia [18]. These approaches are appropriate for digital circuits with discrete signals as they take the discrete transitions as inputs to estimate the power consumption of a given digital device.

Power estimation methodologies of analog circuits which

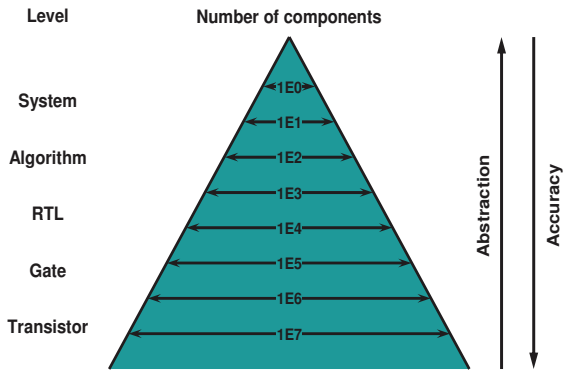


Fig. 2: SOC design levels of abstraction (source [11]) showing that the abstraction decreases, as more knowledge is gained about the SOC. Thus, the power estimation approach after the transistor level presented in this work should be more accurate than the status quo approaches at the system level of abstraction.

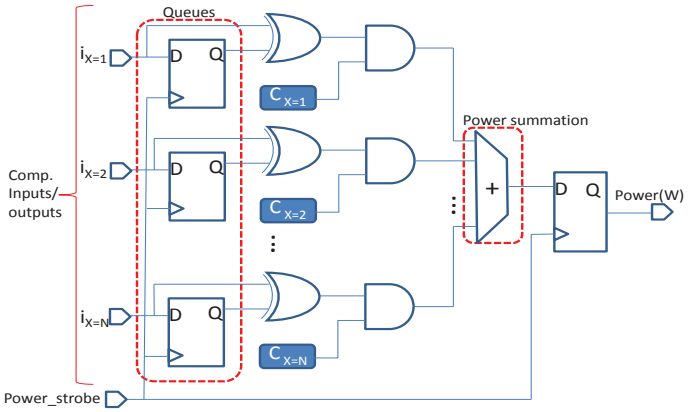


Fig. 3: The power model used for power emulation of digital circuits at the RTL level of abstraction. For a component (RTL gate) of interest, i_x is the value of its input/output. The D and Q values of the flip-flops are the current and previous values of a component's input/output. For each clocking of the power_strobe, the D and Q values are XOR'ed and the product multiplied with the power coefficient C_x to produce the power consumption. The power(W) is the sum of all computed powers for each input/output of the component(s).

are of interest in this work, have been defined at the system level of abstraction [19]–[22]. The methodologies are based on the notion that the estimated power value is the power consumed by a functional block when given relevant input specifications, including the target technology, without knowing the detailed implementation of the block. In this work, we are focusing on power estimation by means of emulation when the first builds of wireless devices (prototypes) with physical layer functionality become available. In contrast to the existing power estimation methodologies for analog circuits, this RF power emulation realistically reflects the wireless device under development, under all scenarios on interest.

Power emulation as a form of power estimation for digital circuits at the RTL level was introduced in [23]–[25]. In this method, illustrated in Fig.3, each RTL component is characterized by a power coefficient C_x which describes the power (in watts) required to charge or discharge the component. These coefficients are given by the specific technology. The power emulated by the model in Fig.3 can be expressed by

$$Power = \sum_{x=1}^{N} XOR(i_x, Q) \times C_x$$

where N is the number of inputs/outputs of the component of interest, i_x is the $x'th$ input/output of the component of interest, Q is the last clocked value of the flip-flop and C_x is the power coefficient of the $x'th$ transition.

To the best of our knowledge, no such emulation models exist for analog circuits. Power estimations for analog circuits have been defined at the system level of abstraction [19] and are based on the notion that the estimated power is the power consumed by a functional block under some specifications such as the specific technology, but without knowing the detailed implementation of the block. The contributions of the work presented in this paper are at a lower level of abstraction, in Figure 2 at the transistor level when the device has been manufactured and a prototype with some minimal physical-layer functionality is available. Therefore, the estimation of power is more precise and reflects the actual hardware properties under various scenarios of interest, for analog RF subsystems in a handset. The approach is to perform the analysis of the logical interface parameters between the RF and BB sub-systems and evaluate their contributions to power consumption. This modeling approach is referred to as Functional Level Power Analysis (FLPA) which follows these steps [26], [27]:

- A primary functional analysis is performed describing the RF subsystem as a grey box with high-level parameters (RF - BB subsystems logical interface parameters);
- hardware power profiling is next performed examining the power consumption when each parameter varies independently;
- power of the RF subsystem is modeled as a function of the defined power relevant parameters;
- a model accuracy computation is performed between the model and the physically measured power consumption.

The rest of this paper is organised as follows:

- The next section (II) covers RF subsystem power emulation followed by homotopies and interval analysis in section III;
- section IV presents the evaluation of the RF subsystem - BB logical interface towards power consumption;
- the RF subsystem power emulation model is presented in section V followed by the discussion and acknowledgements in VI and VII.

II. RF Subsystem Power Emulation

The power consumption of interest in this work is influenced by the type of signal being transmitted. This section discusses the specific signal used, its effect on the BB-RF interface operations and how it can be emulated.

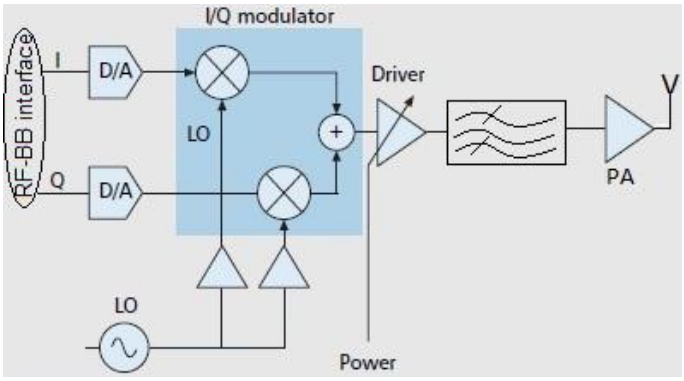


Fig. 4: Direct up conversion transmitter RF subsystem architecture (modified from [28]) of the device used for the experiments in this work. The digital in-phase (I) and quadrature (Q) data from the BB are analog converted, mixed with a RF signal from the local oscillator (LO) and amplified by the PA. The resultant signal is transmitted by the antenna.

A. The LTE handset RF subsystems

Figure 4 depicts the architecture of a direct up-conversion topology of the RF subsystem [28] used for the analysis in this paper. LTE is the newest generation of cellular phone and wireless handset technology and is intended to reach high peak data rates of 100Mbps down-link and 50Mbps uplink (Release 8), low latency, high radio efficiency, low cost and high mobility characteristics [2]. The downlink uses a high PAPR OFDMA, which implies larger power requirements and is thus not suitable for the hand-held handsets. Hence, the handsets use SC-DFMA (Single Carrier-Frequency Division Multiplex access) [29] for uplink transmission. This type of signal determines the protocol related and logical activities between the BB and RF subsystems, which in turn influence the power consumption [30], [31].

The characteristics of the uplink signal defining the logical interface [29] parameters from the LTE technological point of view are:

- the uplink signal bandwidth $\in [1.4\ 3\ 5\ 10\ 15\ 20]$ MHz;
- the modulation (encompassed in the content of resource blocks) schemes QPSK, 16QAM and 64 QAM;
- the TX power of the radio frequency signal (-40 and 23 dBm);
- the carrier frequency f_c (the defined LTE bands).

B. The power emulation methodology

The power emulation system that takes the logical interface parameters between baseband and RF subsystems, via *XTI (X/Open Transport Interface)*, as inputs to compute the sub-frame average power consumption of a specific RF subsystem is depicted in Figure 1.

During run time, the logical interface parameters for each subframe are written to the XTI port in the Tx scheduling function of the modem SW. The trace box forwards the modem software traces to the work station (see Figure 5). The optimal emulation system would compute the emulated RF subsystem power consumption for each subframe in the modem SW and trace it out to the XTI port. However, this approach would increase the CPU load of the modem platform which is undesired.

Therefore, an external approach is taken where the traces are forwarded to the "Parameter extractor" (see Figure 1) module that extracts the logical interface parameters and their corresponding setting times. The "RF power emulator" computes the emulated power $P(t)$ in watts as:

$$P(t) = \sum_{i=0}^{M-1} w_j(t) \times \phi_j(x(t)) \qquad (1)$$

where $w_{j=0\ldots M-1}$ are the RF subsystem power emulation model coefficients, M is the number of coefficients, $\phi(\cdot)$ is the basis function [32] expressing the features of the input digital data $x(t)$ and t is the discrete time in milliseconds.

The next section presents a possible mathematical model for modeling the power coefficients w_j. The emulated power will be a function of many parameters each with a lower and upper bound. The calculation of $P(t)$ for all values of all parameters is prohibitively complex. However, it is possible to reduce this complexity by using an appropriate mapping. For example, $P(t)$ depends on the signal bandwidth, which can be a value between 1.4 and 20 MHz for LTE. Instead of computing $P(t)$ for all intermediate values, we compute it for the limiting ones and apply a mapping called homotopy to obtain all intermediate values. The next section describes this mapping approach.

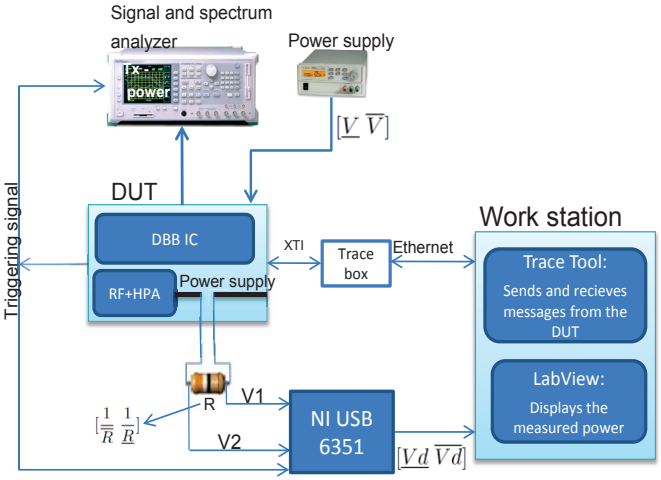


Fig. 5: Power measurement setup used for the measurements in this work. The workstation forces the DUT into a specific mode of operation. During the operation, the DUT power consumption is measured by NI USB and displayed in LabView. The signal analyzer measures the output Tx power at the antenna port

III. Homotopies and Interval Analysis

A homotopy between two continuous functions f_0 and f_1 from a topological space $\mathcal{X}$ to a topological space $\mathcal{Y}$ is defined as a continuous map $\mathcal{H} : \mathcal{X} \times [0,1] \to \mathcal{Y}$ from the Cartesian

product of the topological space $\mathcal{X}$ with the unit interval $[0, 1]$ to $\mathcal{Y}$ such that

$$\mathcal{H}(\mathbf{x}, 0) = f_0, \text{ and} \quad (2)$$
$$\mathcal{H}(\mathbf{x}, 1) = f_1, \quad (3)$$

where $\mathbf{x} \in \mathcal{X}$ is the variable of interest, e.g. the Tx power in our case.

We use homotopies in order to reconstruct the unknown function of the consumed power of several power-influencing variables (logical interface parameters) from measured values. The measurements are obtained by fixing one variable that will be used as the homotopy parameter and varying another variable, or possibly several other variables. In this way, we study the projections of the graph of the consumed power on lower dimensional spaces (usually two-dimensional spaces) corresponding to limit values of the range of the RF subsystem power-influencing variable.

Interval analysis is a well-known method for computing bounds of a function, given bounds on the variables of that function [33]. The basic mathematical object in interval analysis is the interval instead of the variable. The operators need to be redefined to operate on intervals instead of real variables. This leads to an interval arithmetic. In the same way, most usual mathematical functions are redefined by an interval equivalent. Interval analysis allows one to certify computations on intervals by providing bounds on the results. The uncertainty of each measure can be represented using an interval defined either by a lower bound and an upper bound or a midpoint value and a radius. The uncertainty of the consumed power as a function of a variable (say bandwidth) can be represented by an upper bound plot and a lower bound plot. The consumed power in between the measured points can be interpolated linearly or by using cubic splines. The theoretical assumption that the consumed power is monotonically increasing with respect to the defined power-influencing variables is tested by computing the intersection of the areas between the lower bound plots and the upper bound plots corresponding to the limit values of the homotopy parameter.

The non-linear homotopy [34] used here is as follows:

$$H(P_T, \lambda) = \lambda^{\alpha} g(x) + (1 - \lambda)^{\alpha} f(x) \quad (4)$$

where the parameter λ is a function of the lowest and highest signal bandwidth:

$$\lambda = \frac{(BW - 1.4)\text{MHz}}{(20 - 1.4)\text{MHz}} \quad (5)$$

P_T is $[-40\ 23]\, dBm \pm 2dB$, $g(x)$ and $f(x)$ are the power consumptions at $20\, MHz$ and $1.4\, MHz$ respectively. The RF subsystem is assumed to operate in LTE band 1 (1.95GHz) at a bandwidth of 10 MHz.

Figure 6 shows an example of applying homotopy, given by Equation 4, to $P(t)$ with signal bandwidth as a variable. The lower and upper bounds are calculated based on uncertainties in the measurement instruments. The measured curves are obtained by using the setup from Figure 5 at different bandwidths as a function of Tx power. The power consumption is obtained

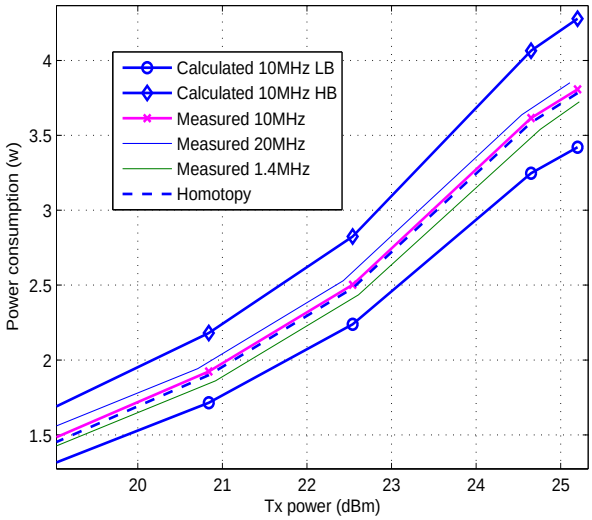


Fig. 6: Homotopical modeling of the RF subsystem power consumption operating at 10 MHz. Only a range of Tx powers is shown for clarity, but the curves are calculated down to -40 dBm.

by measuring the current through the resistor and using the NI USB 6351 instrument to measure the voltage across it. The homotopy curve (dashed line) given by Equations 4 is seen to be in the middle of the range and matches the measured power consumption well.

The relative error between the measured and modeled RF subsystem power consumption is 1%. Further experiments with the modeling of the RF power consumption at operational bandwidths 3, 5 and 15 MHz yielded the same result. Calculations show that the task of measuring the RF subsystem power consumption as a function of Tx power and bandwidth is reduced by 67% by applying homotopy.

IV. Evaluation of the RF - BB subsystem logical interface

A wireless device prototype supporting the LTE technology was used for the analysis of the logical interface parameters towards power consumption. The prototype was connected to a signal analyzer [35] capable of measuring the channel power of the signal at the antenna port.

In order to perform these measurements, the modem platform is forced in a mode referred to as "local mode" where only the physical layer of the modem platform is active. In this mode, it is possible to schedule Tx operations with the desired combinations of the BB-RF subsystem logical interface parameters. The logging of the RF subsystem power consumption and the Tx power on the antenna port is initiated by the triggering signal in Figure 5. The triggering signal is a GPIO (General Purpose Input Output) pin on the modem platform set high for each Tx subframe.

A. Evaluation of the measurement system and methodology

The measurement system is affected by the systematic and random errors arising during the measurement process [36]. The systematic errors are referred to as measurement/instrumental uncertainties and are provided in the manufacturer's specifications for the devices in Figure 5 as:

- voltage supply device (0.05% + 10mV) [37];
- measurement resistor (10%);
- NI USB 6351 (reading × gain error + 10 × offset error + noise uncertainty) [38];
- signal analyzer (0.39dB) [35].

The instrumental uncertainties above are modeled using intervals [33]. The resultant RF subsystem power consumption is thus represented in form of intervals specified by lower and upper bounds:

$$[\underline{P}\ \overline{P}] = [\underline{V}\ \overline{V}] \times [\underline{V_d}\ \overline{V_d}] \times [\frac{1}{\overline{R}}\ \frac{1}{\underline{R}}] \quad (6)$$

where V is the voltage of the source, V_d the voltage measured across the resistor R and the underlines and overlines as in $\underline{V}, \overline{V}$ indicate the lower and upper bounds of the variable V.

The random errors caused by unpredictable variations in the measurement system are eliminated by having the same starting point (trigger) of the measurements and averaging over 1000 subframes for each power consumption measurement.

In order to verify the measurement methodology, three independent data sets of the RF power consumption measurements with the same operational parameters (bandwidth, modulation and carrier frequency) where conducted. Each set of measurements created a buffer zone or offset whose offset parameter corresponds to the absolute value of the measurement uncertainties as shown in Figure 7 (only last box is shown here). Given the three buffer zones in Figure 7, we do have a union and an intersection of the measurements. The Hausdorff distance [39] is used verify how the two sets (union and intersection) differ from each other. The Hausdorff distance measures the similarity of two non-empty compact sets in respect to their position in the metric space. This distance indicates the extent to which each point in the union set is located relative to the points in the intersection set [39]. For a perfect match between measurements, the Hausdorff distance is 0 which would only occur in an ideal setup.

The Hausdorff distance

$$d_{\mathrm{H}}(\cup,\cap) = \max\{\sup_{x\in\cup}\inf_{y\in\cap} d(x,y), \sup_{y\in\cap}\inf_{x\in\cup} d(x,y)\},$$

where $d(x,y)$ is the distance between x the union $\cup$ and y the intersection $\cap$ of the measurement uncertainty boxes is depicted in Figure 7. Here sup is the supremum and inf the infimum. The Hausdorff distance is the length of the straight line segment joining the union and intersection interval boxes at the top right of Figure 7 and is found to be 0.31. The value is acceptable for our purposes but can be reduced in several ways. The simplest and least expensive is to replace the resistor in Figure 5 by one with tighter tolerance.

B. RF subsystem power consumption measurement

The power consumptions of the RF subsystem while operating at 10 MHz in transmit mode is plotted in Figure 8 with its corresponding lower and upper bounds. The lower and upper bounds of power consumption are computed as a function of the uncertainties in the measurement setup. The measured power as a function of the voltage difference over the resistor R has an uncertainty given by:

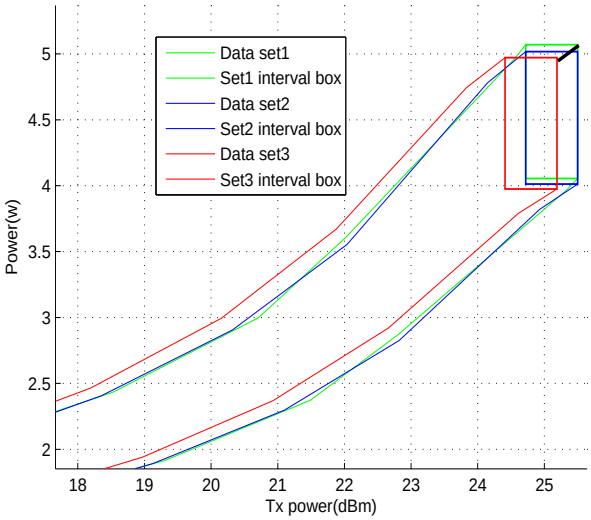


Fig. 7: The buffer zones of three independent measurements used to calculate the Hausdorff distance

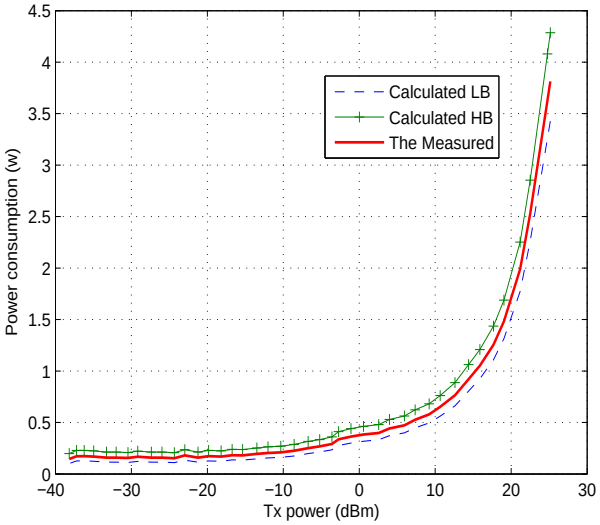


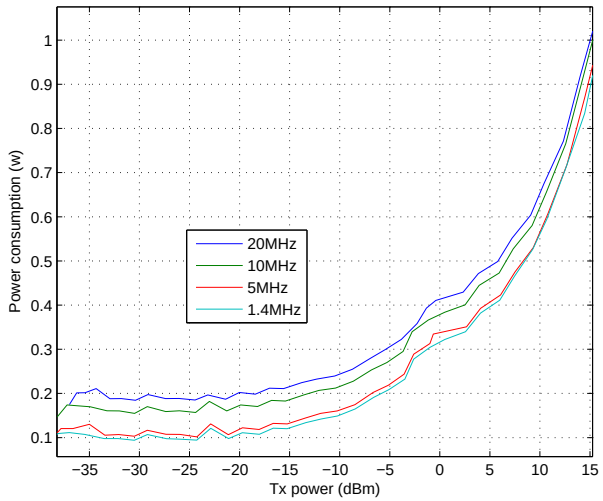
Fig. 8: Measured RF subsystem power consumption operating at 1950 MHz with 10 MHz operational bandwidth and QPSK modulation alongside the calculated lower and upper bounds.

$$\Delta P(V_d) = \frac{(\Delta V \cdot V_d + V \cdot \Delta V d) \cdot R + V \cdot V_d \cdot \Delta R}{R^2} \quad (7)$$

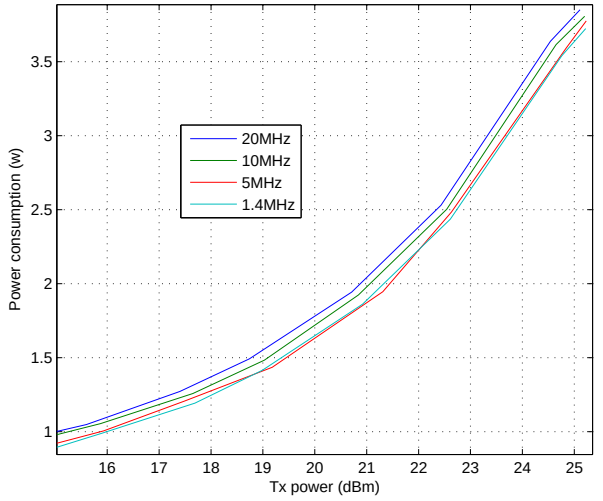
Figure 9 depicts the power consumption of the RF subsystem in transmit mode as a function of the LTE operational bandwidth. The power consumption shown in Figures 8, 9 and 11 is measured for the transmitter terminated in a 50Ω load.

V. RF SUBSYSTEM POWER EMULATION MODEL

The emulation model for each RF subsystem is gained through the process illustrated in Figure 10. For every modem platform with a new RF subsystem design, a mathematical model for its power consumption is obtained via the FLPA analysis. The mathematical model for the RF subsystem used in this work was obtained in [40] where it was also proven



(a)



(b)

Fig. 9: Power consumption vs. bandwidth and Tx power for two ranges: (a) $[-40\ 15]$ dBm and (b) $[15\ 23]$ dBm

that its the carrier frequency, signal bandwidth and Tx power that do have a relevant impact on power consumption and thus make up the inputs for the power emulation system. In this section, the emulation model applied in the power emulation system is described, its validation and the illustration of the emulation system utilization.

A. Emulation model

An evaluation of multivariate modeling approaches towards an approach with the least relative error between the measured and modeled RF subsystem power consumption was performed in our previous work [40]. The approaches in the evaluation were multivariate polynomial fitting and neural networks applying gradient descent, Pseudo-Gauss-Newton and Conjugate gradient algorithms (Hestenes-Stiefel, Fletcher-Reeves and Polak-Ribiere) for optimization. The $4 \times 5 \times 1$ neural network applying Pseudo-Gauss-Newton approach for optimization proved to have the highest mathematical approximation accuracy of 94.03%. Thus, the hidden and output

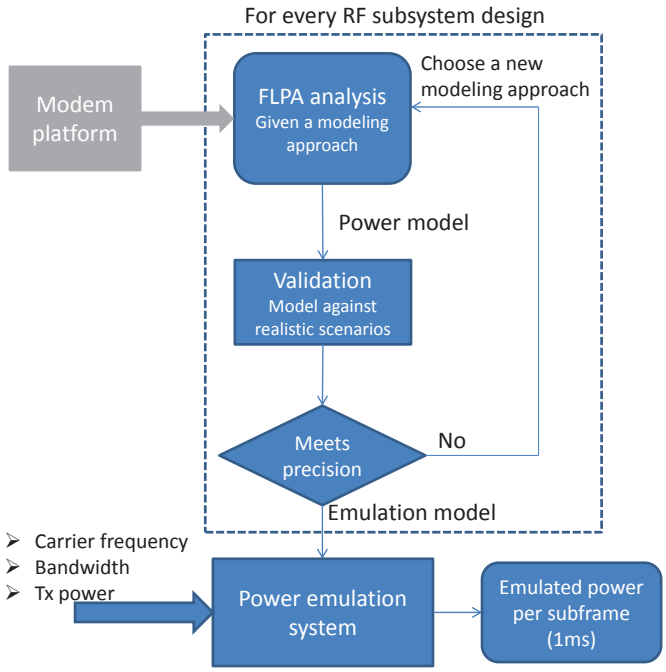


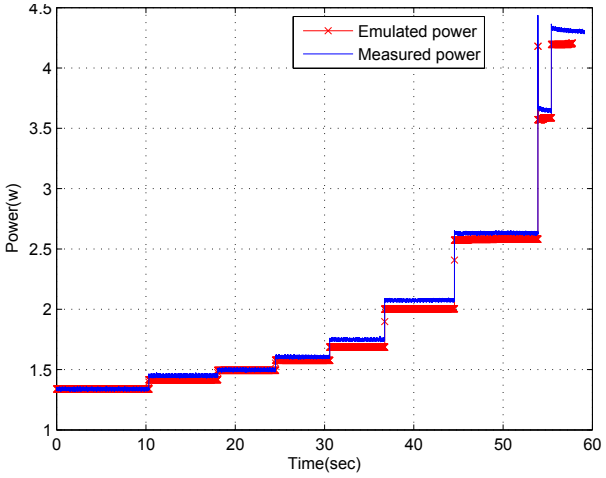
Fig. 10: Emulation flow showing the process through which the emulation model of a RF subsystem is obtained.

unit coefficients of the neural network do make up the RF subsystem power emulation model of the DUT.

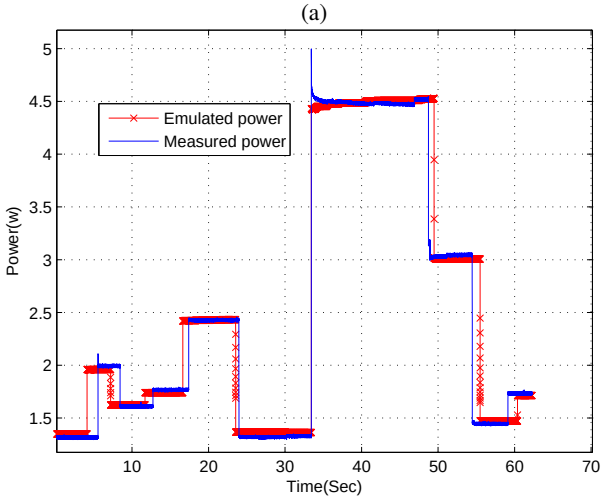
B. RF Power emulation validation

The RF subsystem power emulation model in [40] was trained in a mode when only the physical layer of the modem platform is active. Hence, the RF subsystem power emulation model has to be validated in a "normal mode" when the entire modem platform is active. In order to accomplish this, the signal analyzer in the "Power measurement setup" (see Figure 5) is replaced with a *System Simulator (SS)* which simulates the base-station. The RF subsystem power emulation model is hence validated through the following steps:

1) two test cases as functions of Tx power at a carrier frequency of 1950 MHz, signal bandwidth of 10 MHz and QPSK modulation are invoked in the SS while measuring the voltage difference across the measurement resistor (Figure 5) and logging the modem SW traces. In scenario 1, the Tx power is gradually increasing as in the realistic scenario when a UE is synchronized with a base-station and in scenario 2, the Tx power is randomly alternating to challenge the model but never happens in realistic scenarios;
2) the modem SW traces are extracted for the BB-RF subsystem logical interface parameters, carrier frequency, bandwidth, modulation and Tx power;
3) the outputed power of the neural network is computed as illustrated in [40];
4) the relative error between the emulated power and measured power is evaluated (Figure 11).



(a)



(b)

Fig. 11: Power emulation validation: (a) Tx power increasing between $[-6\ 23]$ dBm and (b) randomly alternating Tx powers

In Figure 11, the measured and emulated power consumption of the RF subsystem is shown, for Tx power increasing from -6 to 23 dBm in Figure 11a and for randomly alternating Tx power in Figure 11b. The relative error between the measured and emulated power of the RF subsystem is 5.77% for the Tx increasing scenario and 11% for the randomly alternating Tx power scenario (which is disregarded). The 5.7% modeling error can be guarantied if the uncertainty in the measurement setup, used for training the emulation model, is $\leq$ 5.19%. A revision of the measurement setup indicates that by using a the measurement resistor with tighter tolerance resistor of $\leq$ 4.2%, the emulation error of 5.77% can be guaranteed.

For more realistic validation, an external antenna was connected to the antenna port instead of the system simulator and the DUT was registered on the Telia network Denmark. A *FTP (File Transfer Protocol)* upload was conducted while measuring the power consumption of the RF subsystem. The measured and emulated power of the FTP upload scenario also had relative error of 5.77%.

C. RF Power emulation illustration

The target of this work is to estimate the RF subsystem power consumption of wireless devices in real life scenarios at an early stage of the production process for the purpose of optimization. The power consumption estimate, of the RF subsystem of the DUT, for a FTP upload scenario when the DUT is in motion is obtained through the following steps:

1) flash an existing LTE wireless device with the modem SW used by the DUT for computing the emulation model;
2) connect the device to a trace box via XTI port, start logging the modem SW traces and connect the device to a cellular network;
3) put the device in a car, start driving and conduct an FTP upload;
4) save the modem SW traces and perform steps 2 and 3 from the validation section to compute the emulated power in Figure 12.

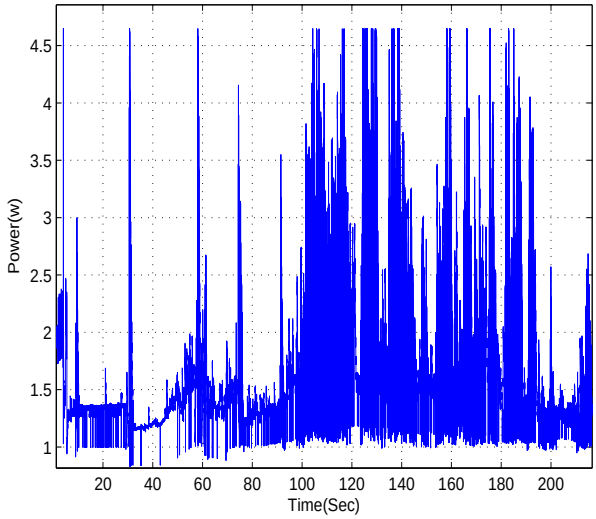


Fig. 12: Emulated power of the DUT during a FTP upload when the device is in a moving car

Even though the prototype (DUT) used for training the emulation model is not capable of conducting a FTP upload, the emulated power gives an estimate $(\pm 11\%)$ of its power consumption for a FTP upload in motion. Thus, with this methodology, we can have an insight in the RF subsystem power consumption for all scenarios of interest given the modem SW traces.

VI. Discussion

In summary, this work presents a new emulation methodology for the analog RF subsystem in a portable device, focusing on the LTE transmitter. The emulated power is computed as a function of the logical interface parameters using a predefined emulation model. The model was shown to have a modeling error of 5.19%, and was obtained via a $4 \times 5 \times 1$ neural network with a Pseudo-Gauss-Newton optimization algorithm. A validation in a realistic scenario shows a accuracy of 94.3%, which can be guaranteed if the measurement uncertainty is

less than or equal to the emulation modeling error. Ongoing extensions of this work include:

- emulation models that incorporate effects of the physical environment resulting in antenna mismatch;
- emulation of Specific Abs Rate (SAR) in parts of the human body loading the antenna and
- topology and architecture dependent power emulation model.

The emulation method and results presented here focuses on the RF transmitter portion because, historically, the PA was the largest power consumer in a portable device. However, in the newest smartphones, such as e.g. the Samsung Galaxy S III and its predecessor [41], dual and quad core Gb/s speed processors required for high-data rate applications start dominating the power consumption and heat removal requirements. The power consumption of these processors can be emulated by power estimation tools such as PowerTheater [15] given their RTL codes. This approach applied to realistic scenarios would have enormous memory requirements, and thus is inefficient. The approach presented in this paper can also be applied to the emulation of power consumption of the application processors under realistic operational scenarios.

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