A Low Phase Noise Multi-Gigahertz Ring based Voltage-Controlled-Oscillator in 0.13 μm CMOS Technology

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Abstract—in this paper, a low phase noise and low supply voltage ring based voltage-controlled-oscillator (VCO) is presented. The phase noise performance is improved by modifying the symmetrical load differential VCO delay-cell structure in order to maximize the output voltage swing. The circuit is implemented in a 0.13μm CMOS technology. The operation frequency of the proposed ring based VCO is from 6138 to 7222 MHz. The characteristics of the proposed ring based VCO are −128.2 dBc/Hz at 1 MHz frequency offset in terms of phase noise, and 2.42 mW with a 1.2 V voltage supply in terms of power consumption.

Index Terms— Phase noise, ring oscillator, delay cell, symmetrical load, output voltage swing, voltage-controlled oscillator (VCO).

I. INTRODUCTION

THE oscillator constitutes a major part of many electronic systems, ranging from the clock generation circuit in the microprocessor to the carrier synthesis in the cell phone, where the required structure and performance parameters vary widely. This article deals with CMOS oscillators, acting in a Voltage controlled oscillator (VCO).

For the VCO's conventional design, there are many performance parameters to consider, including the center frequency, the voltage swing, the regulation range, the frequency adjustment, the linearity, the power consumption, power supply and the common mode rejection.

In addition, the designs of oscillators must be based on functional requirements and related performance indicators, including noise suppression and chip area. The chip area issue can be of great handicap in the LC based VCO design despite its good performance in terms of noise suppression.

On the other hand, a ring based VCO can be implemented integrally in CMOS technology, where there is absence of inductance components. This absence saves a lot of chip area. In fact, this is one of the major advantages of ring based VCO because it permits the achievement of low-cost voltage-controlled oscillator. In addition the implementation of the VCO in the CMOS technology makes the VCO tuning range wider compared with VCO in other technologies [1].

In this paper, the phase noise of differential ring oscillators is improved using a new design, making the VCO competent with LC designs. The design was implemented in a standard TSMC 0.13μm CMOS process, with oscillation frequencies up to 7.222 GHz.

In section III, the architecture of the symmetrical load differential VCO delay cell structure is examined. Also, the use of the two-tailed current sources and the self-excited tube structure and their impact on the increase of the oscillation frequency and the voltage swing at the output are examined. In Section IV, the design of the proposed VCO is described. In addition, the measurement results of this VCO are presented. At the end of this section, the results are compared with other published works.

II. PHASE NOISE IN RING OSCILLATOR

Timing uncertainty of a periodic signal is either referred as phase noise or jitter. Phase noise and jitter are used to measure the oscillator noise performance parameters. While phase noise is the uncertainty in the frequency domain used to measure the spectral density of the oscillator, jitter is used to define the uncertainty in time domain [2]. Thus, they refer to the same phenomenon, and phase noise will be used to refer to both through this dissertation in qualitative discussions.

The ideal oscillator output spectrum is a pulse function, but due to various noises in the circuit resulting from the temperature variation, power supply voltage and other factors, the output signal spectrum will change as shown in Fig. 1.

The factors that contribute to the phase noise can be classified in two categories. First, the random factors that create random variations of the timing of the signal edges. Major part of this noise originates from thermal noise and flicker noise (1/f noise) of active and passive devices that constitute the circuits. Note that at temperatures higher than absolute zero, every active and passive device in a circuit exhibit thermal and flicker noise.

Fig. 2 shows the different areas of phase noise. Area $1/f^2$ due to thermal noise and area $1/f^3$ due to low frequency noise are considered as flicker noise in MOS devices. Note that "f" is considered as the carrier frequency.

Reducing all these components of the phase noise to some level is possible using different circuit design techniques. However, its effect is fundamental and it is often the major contributor of the total phase noise.
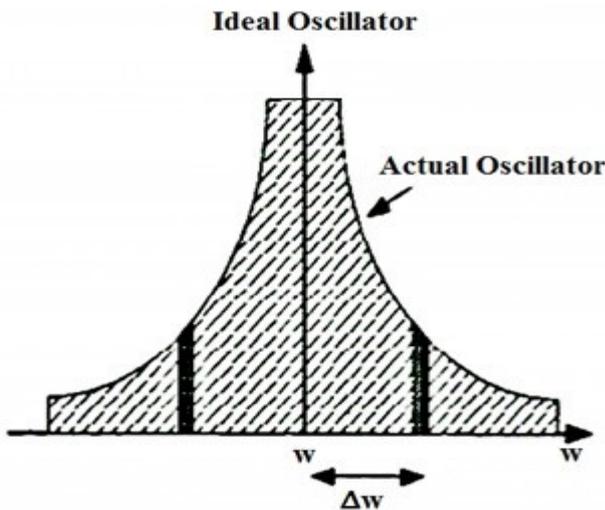
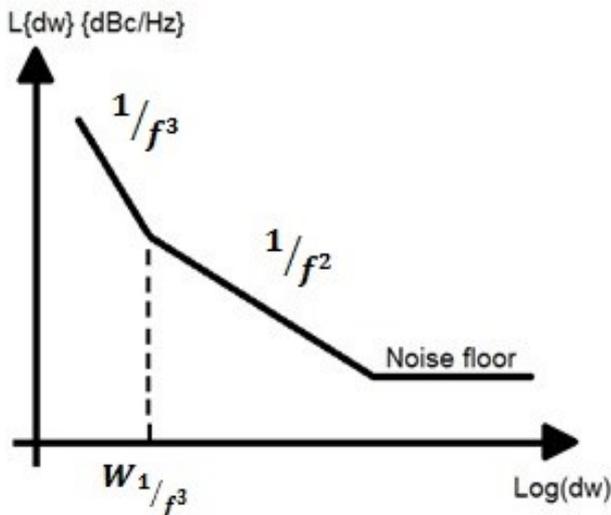Fig. 1. Oscillator spectrum in frequency domain

Fig. 2. Different regions of phase noise

The second category contributing in the phase noise is the system factors that can generally be avoided by a careful design of the system. This noise is caused by interfering signals from other parts of the integrated system, usually the power supply and ground lines.

Of course, inputs of system components, such as the control input of an oscillator, are also susceptible to this kind of disturbance. The effect of mismatches between devices and the delays of different oscillator stages is also considered to be part of the system factors.

In general, there are various methods available to reduce the output noise of a ring oscillator. Some of these methods are intended to lower the effect of a specific noise source while others improve the overall noise characteristics of the circuits.

Additional techniques to decouple the circuit from the power lines along with the differential architecture are implemented in case the power lines are the most significant noise sources in the system.

III. SYMMETRICAL LOAD DIFFERENTIAL VCO WITH TWO-TAILED CURRENT SOURCES AND SELF-EXCITED TUBE STRUCTURE

Because of the frequency limitations and low phase noise performance of a single-loop based ring oscillator, other architectural techniques are necessary to reach lower levels of phase noise in ring oscillators.

The swing enhanced structure which is shown in Fig. 3 (a) is the architecture chosen in this work, for a 3-stage ring oscillator as shown in Fig. 3 (b).
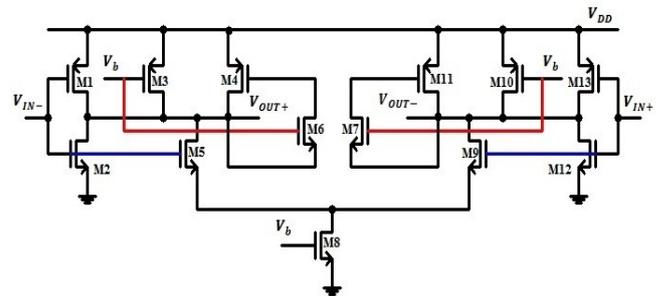
(a)
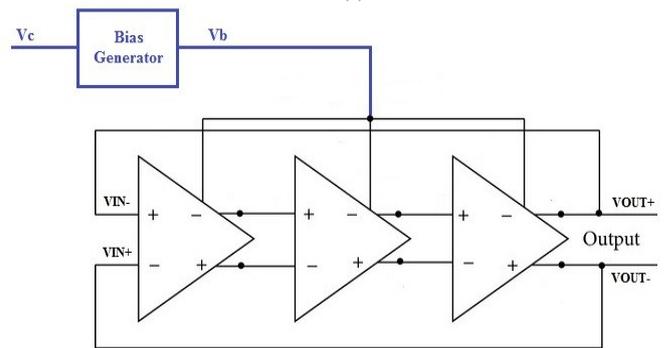
(b)

Fig. 3. Proposed (a) delay cell and (b) 3-stage ring oscillator

This technique adds two-tailed current sources while uses a self-excited tube structure to design new differential VCO extension. The main idea is to eliminate the disadvantages of symmetrical load differential VCO, and play to their strengths, to design a new extension delay unit configuration, so that a cascade of 3 stages of these units constitute a High Performance Voltage-Controlled Oscillator (HPVCO), characterized by a stable full-swing output with a wide range of voltage regulation.

A. Swing Lifting Structure

First, in order to improve the symmetrical load differential VCO, it is necessary to eliminate the correlation between the output signal amplitude and the control voltage (V_c) changes. This shortcoming of the based symmetrical load delay unit circuit structure is fixed by the addition of a pair of MOSFET (M1 and M2 in the Fig.3 (a)) to construct a Swing-Enhanced Structure (SES).

This structure is similar to the inverter structure, mainly used to enhance the output signal swing. This Structure achieves an output signal swing that does not change with the control voltage (V_c).

The use of a SES introduces a new current that may cause the tail current throw M8 to change and thus changes the output frequency.

In the design process, there is a need to match the width size of M1 (pMOS) and M2 (nMOS), so the tail current flow is not affected. In fact, the movement of holes in semi-conductors is slower compared with that of electrons. Thus, in order to deliver the same current as nMOS transistor, a pMOS transistor must have a greater width. Thus, the ratio of width over length W/L of pMOS is taken as 3 times the one of the nMOS to guarantee the current condition.

As for the frequency control, when the bias voltage V_b is greater than 0.7V, the tail current source (M8) is activated, and the symmetrical load differential circuit structure starts to work, so that the frequency of the output signal starts to change with the control voltage V_c and directly with the bias voltage V_b.

B. Double Tail Current Source Structure

On the basis of the symmetrical load delay unit circuit structure, the introduction of the swing lifting structure effectively improves the signal swing. VCO voltage swing is lying between 0 volt and the supply voltage level, but it is assumed that when the bias voltage V_b is low, the differential VCO frequency is not controlled by the control voltage V_c.

The reason for this is that when the control voltage V_b is low, the tail current throw (M8) is in the cutoff region or the linear region, resulting in symmetrical load differential circuit that is not working properly.

In order to eliminate this phenomenon and to ensure that the differential VCO output signal is in the control voltage full range of changes, a (Dual Current Structure, DCS) is introduced, to ensure a symmetrical load differential circuit is working properly.

Due to the introduction of DCS, the SES has little effect on the output frequency, and its main role becomes the amplification of the output swing. In consequence, the amplitude of the output swing variation with the control voltage Vc greatly reduces. Note that, the role of the DCS is to increase the frequency of the output signal, and to ensure that the two differential outputs of the VCO are 180 degrees out of phase.

C. Self-excited Pipe Structure

After adding the swing lift structure and the double-tailed current source structure, the benefits are increased, but to the detriment of gain reduction which means that the VCO adjustment range is reduced.

In order to maintain the advantage, the gain should be increased to maintain linearity at large or full range of control voltage. This is solved by introducing a self-excited tube junctions (Incentive Transistor Structure, ITS). In the proposed design M6, M7 play the role of the new self-excited tube.

Concerning the operation of the self-excited tube, when the differential input V_{IN-} is low, the differential output V_{OUT+} is high and the control voltage V_c is fixed at a certain value. The source of M6 is at high potential, the drain is connected to the gate of M4 , and the drain potential is low, since the two-stage source of the transistor can be interchanged, M6 draws current

from V_{OUT+}, and charges the gate of M4, resulting in M4 charge current decreases.

When the differential input V_{IN-} is high, the differential output V_{OUT+} is low, M6 discharges from the gate of M4 to V_{OUT+}, making the M4 gate potential decreases, resulting in M4 charge current to increase. The self-energizing tube (M6) functions as a negative feedforward, effectively adjusting the linearity.

IV. OSCILLATOR DESIGN RESULTS

The proposed ring based VCO is simulated in a 130 nm CMOS technology.

In Fig. 4, is showed the variation of oscillation frequency obtained versus the variation of bias voltage. In response to a sweep of the bias voltage between 0.7 and 1.2 V, the operation frequency increases progressively from 6138 to 7222 MHz.
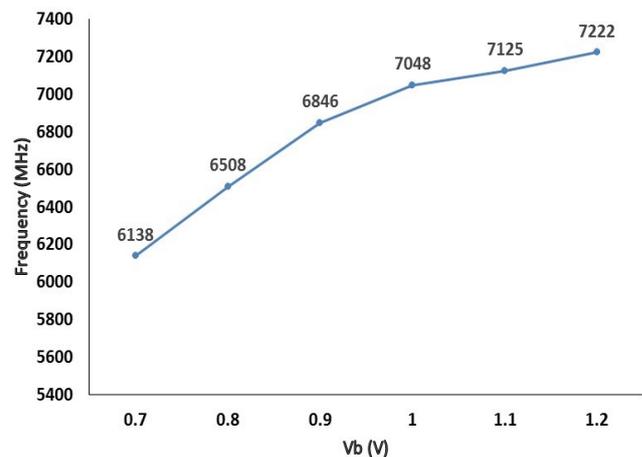

Fig. 4. Measured oscillation frequency of the proposed VCO versus the bias voltage.

Fig. 5 shows the transient response of the proposed based VCO. The voltage swing is limited between 0.3 and 1.15 V.
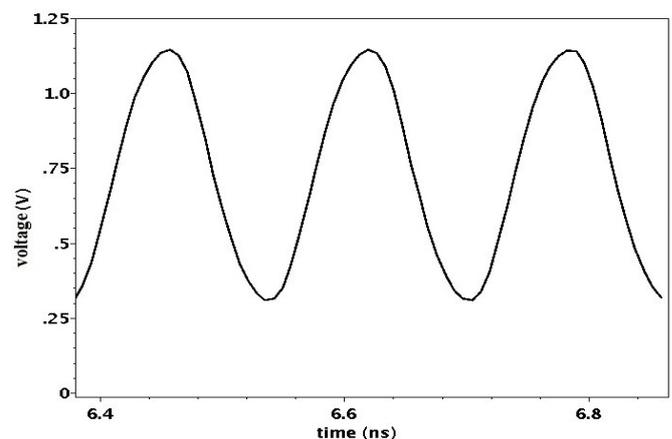

Fig. 5. Output transient response

As shown in Fig.6, the measured phase noise is −128.2 dBc/Hz at a 1MHz offset at an oscillation frequency of 6138 MHz while the power dissipation is 2.42 mW at a 1.2 V supply.
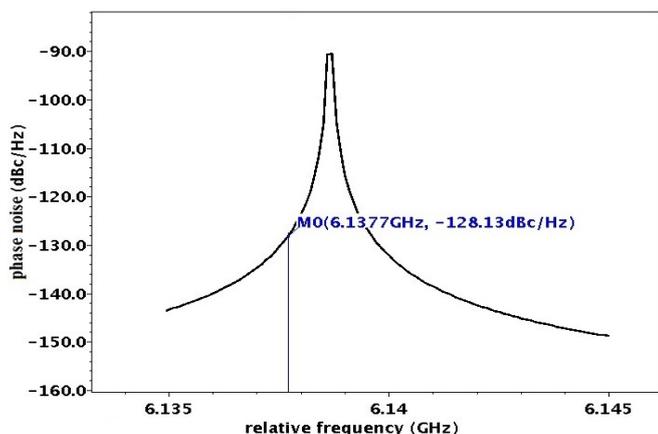
Fig. 6. Phase noise measured at 1 MHz offset

The phase noise of the proposed VCO is 20 dB lower than that in [7] for the same basic design structure and at the same frequency offset.

Table I shows a comparison of the measurement results of the proposed VCO with results of other works. Any comparison should be based on clear criteria. Because the results of different works have different frequencies and power consumptions, a figure of merit (FoM) is defined below [8]:

$$FoM = -20 \log \left(\frac{f_0}{\Delta f} \right) + 10 log \left(\frac{P_{dc}}{1 \ mW} \right) + L\{\Delta f\} \qquad (1)$$

In Equation (1), $L\{\Delta f\}$ is the phase noise from the oscillation frequency (f_0), Δf is the offset frequency from the carrier and P_{dc} is the power consumption of the VCO.

TABLE I
PERFORMANCE COMPARISON WITH OTHER VCOs

Ref.	Process (nm)	Supply (v)	P_{diss} (mW)	f_{osc} (MHz)	Phase Noise @ 1 MHz (dBc/Hz)	FoM (dBc/Hz)
[3]	500	2.5	15.4	900	-105@600KHz	-157.1
[4]	600	3	30	900	-117@600KHz	-165.7
[5]	180	2	22	630	-108	-150.6
[6]	180	1.8	13	1861	-102	-156.3
[1]	180	1.8	N.A	5790	-99.5	-
This work	130	1.2	2.42	6138	-128.2	-200.12

V. CONCLUSION

A low phase noise and low voltage ring based VCO is proposed as a promising structure in CMOS integrated technology. The performance of the phase noise is improved by modifying the symmetrical load differential VCO delay cell structure to extend the output voltage swing. The VCO is implemented in a 130 nm CMOS technology. The new structure has a frequency tuning range from 6138 to 7222 MHz (about 17.66%). At 6138 MHz, the measurement shows that the phase noise is −128.2 dBc/Hz at frequency offset 1MHz with a power dissipation of 2.42 mW at a 1.2 V supply. Regarding the FoM, the VCO proposed in this work scored −200.12 dBc/Hz. The VCO proposed provided an optimized design to achieve low phase noise for low supply voltage in the deep sub-micron technology.

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