Amorphous Silicon Thin-Film Transistors based Digital Circuits

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ABSTRACT

This paper is concerned with the implementation of an amorphous silicon based thin-film transistor model and with amorphous silicon technology as an alternative technique of the implementation of digital circuits. The model reliability is validated by the investigation of amorphous silicon based NAND and NOR gates. The characterization includes high and low logic levels and propagation delay. The obtained results are presented and demonstrated to be reliable and strongly governed by simulation parameters. The results may serve as a foundation for amorphous silicon logic circuits design.

KEYWORDS

Amorphous silicon, a-Si:H TFT, a-Si NAND gate, a-Si NOR gate, logic design.

1 INTRODUCTION

Since plasma-enhanced chemical vapor deposition dielectrics and hydrogenated amorphous silicon (a-Si:H) can be deposited at low temperatures on large-area substrates, hydrogenated amorphous silicon thin-film transistors (a-Si:H TFTs) have a wide range of applications. These TFTs have become the most widely used switching devices for active matrix liquid crystal displays (AMLCDs) as well as other applications. Possible improvements in amorphous silicon technology depend, not only on the understanding of device physics but also on the adequate modeling of the electronic transport phenomena of materials. Thus availability of coarse and simple analytical models that can grasp the physical phenomena of a-Si:H TFTs and concisely formulate their characteristics are particularly attractive. These models must be aimed at lessening the cost and complexity in fabricating large-area displays and optimizing their performance. The published developed models described the behavior of hydrogenated amorphous silicon based TFTs under external constraints [1], [2], [3], and have shown that optimal design and fabrication of reliable a-Si circuits require confirmation of robustness and efficiency of the simulation based optimization. This may help to achieve superior stability and feasibility [4]. In fact, simulation is one of the important concerns for integrated circuits design flow. Many attempts have been made to verify the functionality of such circuits and insure the validity of the functions they generate by simulations.

This paper deals with the use of LTspice simulation software [5] to implement an a-Si:H TFT model for integrated circuits design. It aims to develop and investigate the feasibility of building a-Si based digital circuits. In applications such as AMLCDs, a-Si:H TFT logic circuits design seems attractive since as soon as a-Si switching array is fabricated, the design of these circuits comes into question. So, once the operation and characteristics of these circuits are thoroughly understood, the results can be extended to the design of more complex blocks. Such study is provided in this paper for amorphous silicon based NAND and NOR gates. I will try to take a more comprehensive look at these circuits, investigating their performance and exploring the trade-offs available in their design. This may serve as a foundation of the design of a-Si logic circuits. For this purpose, a standard integrated circuit

design flow was adopted to set up the representative model of the transistor as indicated by Fig. 1. The simulation software offers several features and analyses. One of its major advantages is the possibility it offers to implement components models and incorporate them to build more complex circuits.

The organization of this paper is made as follows: Section two describes the model implementation and introduces background knowledge of the used a-Si:H TFT model and related modeling of the electronic transport phenomena. Section three presents the model validation before conclusion is drawn.

2 MODEL IMPLEMENTATION

In LTspice, implementing a model needs the creation of a symbol and a library for the component. The symbol is a graphic file (.asy file). The library specifies the electric connections and the model composition (.txt or .lib file). In the present work, a TFT model was created to which a TFT.asy symbol and a TFT.lib library were associated. The generated new component will be exportable into other schematics provided to include the representative functioning library. This step is very important. It enables a link between the symbol and the model. The adopted electrical model for this study is illustrated on Fig. 2. It describes the static and the dynamic behavior of the studied transistor's structure [6], [7]. In [6], a dc model for a-Si:H TFTs including an accumulation region is developed. The model describes the device properties and physical phenomena of hydrogenated amorphous silicon. Current-voltage characteristics are related to basic material and device parameters. In the blocking state drain leakage current is modeled using previously reported results. Below and above the threshold operation both deep and tail states are taken into account. The density of states in the band-gap is modeled by assuming an exponential distribution of the deep and tail states. In [7], is presented an analysis that considers the channel charge and its transient characteristics using the charge oriented model. The gate-to-source capacitance C_{gs} is the contribution of the overlap gate-to-source capacitance C_{gso} due to geometrical effects between the source-gate metal layer and the intrinsic gate-to-source channel capacitance C_{gsi}. Similarly, the gate-to-drain capacitance C_{gd} is the contribution of the overlap gate-to-drain capacitance C_{gdo} due to geometrical effects between the drain-gate metal layer and the intrinsic gate-to-drain channel capacitance C_{gdi}. I_d is the current source generated by the TFT drain. It describes the subthreshold and the above threshold regimes in a-Si:H TFTs and presents the physics of a standard planar a-Si:H TFT with lateral current flow from source to drain. I_d is found to have the following expression [6]:

$$I_d = \begin{cases} f_t(T_d, \mathrm{T_t}, \mathrm{T})(V_g - V_t)V_d \text{ for } \mathrm{V_d} << \mathrm{V_g} - V_t \\ \frac{1}{2} f_t(T_d, \mathrm{T_t}, \mathrm{T})(V_g - V_t)^2 \text{ for } \mathrm{V_d} \geq \mathrm{V_g} - V_t \end{cases} \quad (1)$$

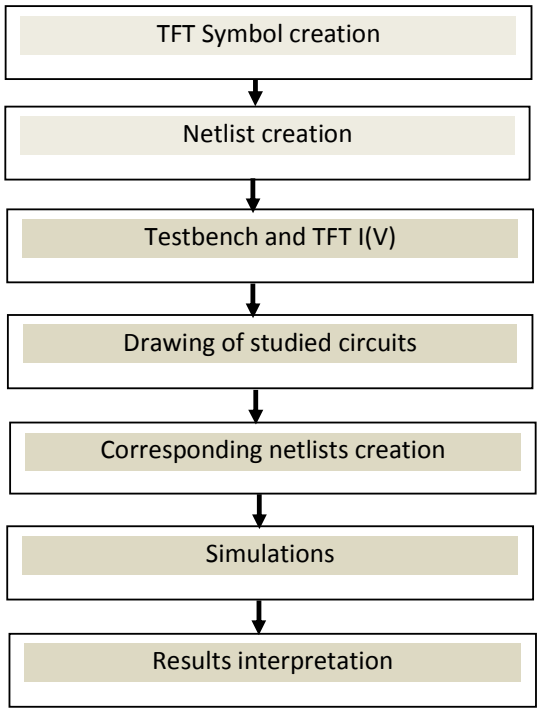


Figure 1. Approach followed in this work.

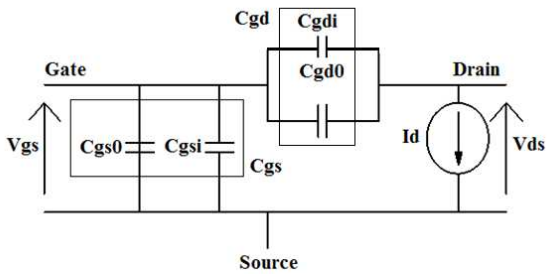


Figure 2. Adopted TFT model.

where V_d and V_g are drain and gate voltages, respectively, I_d is the drain current, V_T is the threshold voltage, and f_t is expressed as:

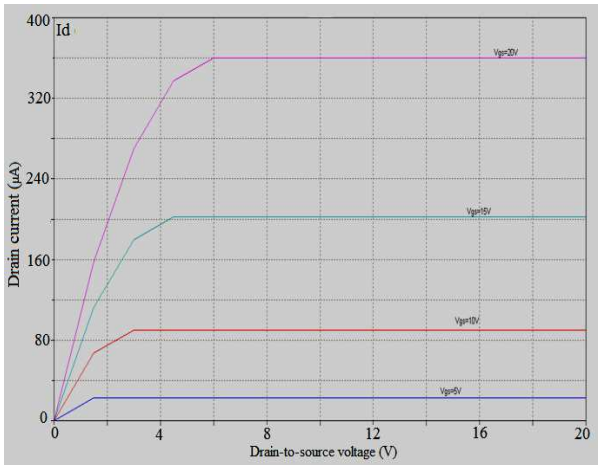
$$f_t(T_d, T_t, T) = \frac{Z\mu_n N_c C_i}{LkT\left(\frac{gg_d}{T/T_d - 1} + \frac{ggt}{T/Tt - 1} + \frac{N_c}{kT}\right)} \quad (2)$$

where Z and L are the width and the length of channel, $C_i=\varepsilon_i/d$, where ε_i and d are the insulator dielectric constant and thickness, respectively, is the insulator capacitance per unit area, N_c is the effective density of states in the amorphous silicon, μ_n is the electron mobility, g_d and g_t are the deep states density and the tail states density at the conduction band edge, E_c, respectively. T_d and T_t are characteristic temperatures for the deep states and the tail states, respectively. k is the Boltzmann's constant, T is the absolute temperature and g is the degenerescence factor of the acceptor-like states. The used parameters for the transistor under study are summarized on table 1.

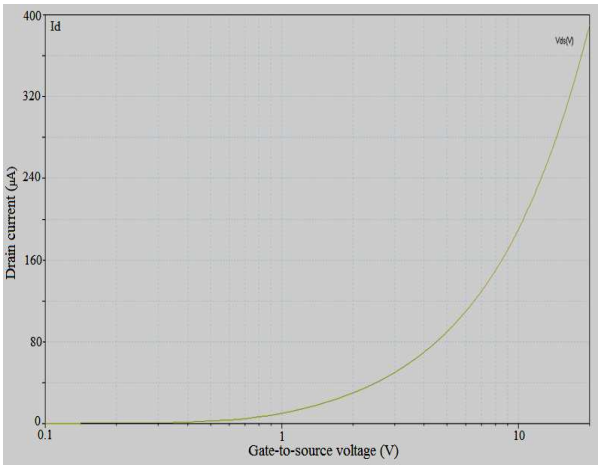
Table 1. a-Si:H TFT parameters used in the simulations.

Band mobility	8 cm^2/Vs
Channel length	8 µm
Channel width	80 µm
Effective density of states	$7x10^{19}$ cm^{-3}
Deep states density at $E=E_c$	$8.8x10^{18}$ $cm^{-3}eV^{-1}$
Tail states density at $E=E_c$	$2.1x10^{22}$ $cm^{-3}eV^{-1}$
Characteristic temperature for deep states	1000 °K
Characteristic temperature for tail states	260 °K
Bulk Fermi level	0.65 eV
Insulator thickness	3000 Å
a-Si:H dielectric constant	$1x10^{-12}$ F/cm
Insulator dielectric constant	$6x10^{-13}$ F/cm
a-Si:H gap	1.72 eV
Temperature	300 °K
Insulator fixed charges	10^{10} cm^{-2}
C_{gs0}	0.1pF
C_{gsi}	0.1pF
G_{gd0}	0.1pF
C_{gdi}	0.1pF

For TFT simulations, the created test bench allowed for the investigation of the transistor I-V characteristics. Typical transfer and direct characteristics are shown on Fig. 3.



(a)



(b)

Figure 3. LTspice direct (a) and transfer (b) characteristics of the TFT under study.

As can be seen, the obtained results suggest the well known dependence of these characteristics on external applied voltages.

3 MODEL VALIDATION

To validate the implemented TFT model with LTspice, the behavioral study of an amorphous silicon based NAND and NOR gates was investigated. The configurations used for these gates are shown on Fig. 4. Since only NMOS devices can be fabricated in a-Si technology, the circuits utilize basic configurations which consist of input transistors driven by input voltages and, instead of integrated ohmic load resistors, enhancement NMOS a-Si:H TFTs as load devices which are diode connected are used. The biasing voltage is V_{dd}. The input signals are used to be bipolar pulses which vary from 0V to 20V. The input pulse widths are deliberately made different to investigate the functionality of the gates. The transient simulation tests were run on V_{dd} value of 20V. They revealed, as shown on Fig. 5, that the model reproduces well the representative truth tables of NAND and NOR gates.

The validation of the TFT model implementation was also used to investigate the gates performance. The characterization step includes the trends of the delay propagation and the high and low logic levels when the supply voltage varies from 5V to 20V. Figures 6 and 7 illustrate these trends for NAND and NOR gates, respectively. As was expected, the implemented model predicts the rise of the above mentioned parameters when the supply voltage increases. The evolution of high and low levels is crucial because it is directly related to the noise immunity of the two gates. These circuits reliably work when the noise margin is sufficiently high. As this parameter is closely related to their input-output voltage characteristics, the mentioned figures suggest that the gates outputs are strongly affected by increasing the supply voltage. The noise at their

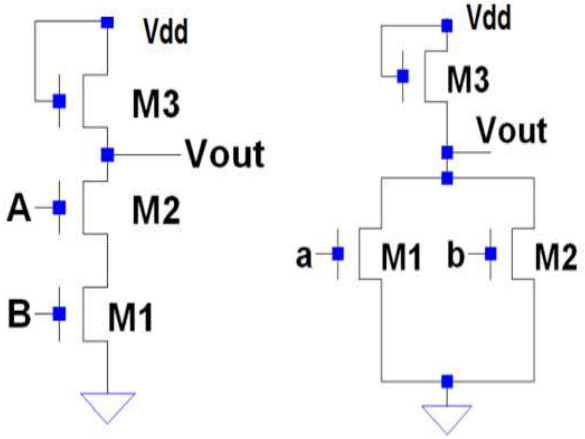
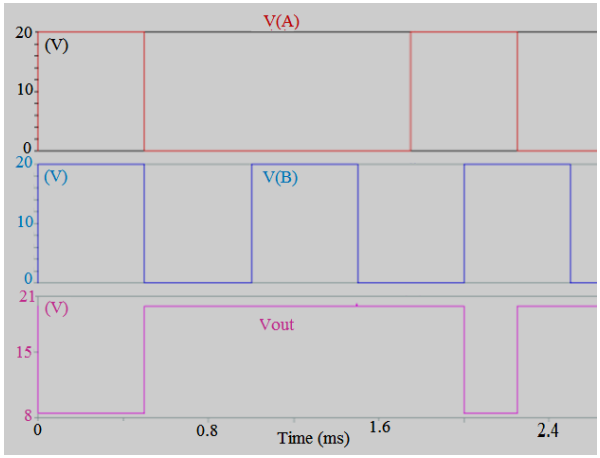
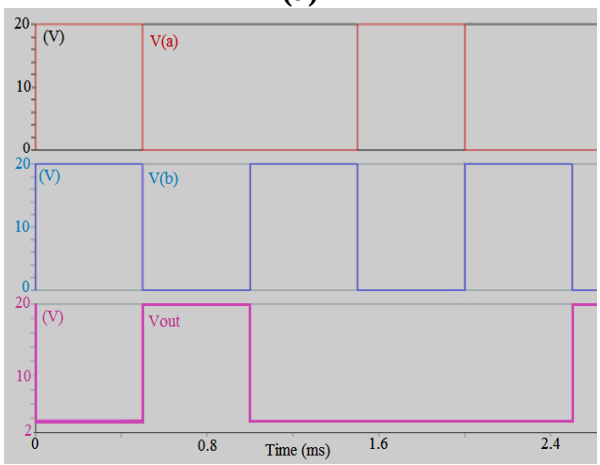


Figure 4. a-Si NAND gate(a) and a-Si NOR (b) gate configurations.



(a)



(b)

Figure 5. Obtained LTspice timing diagrams for a-Si NANd (a) and a-Si NOR (b) gates.

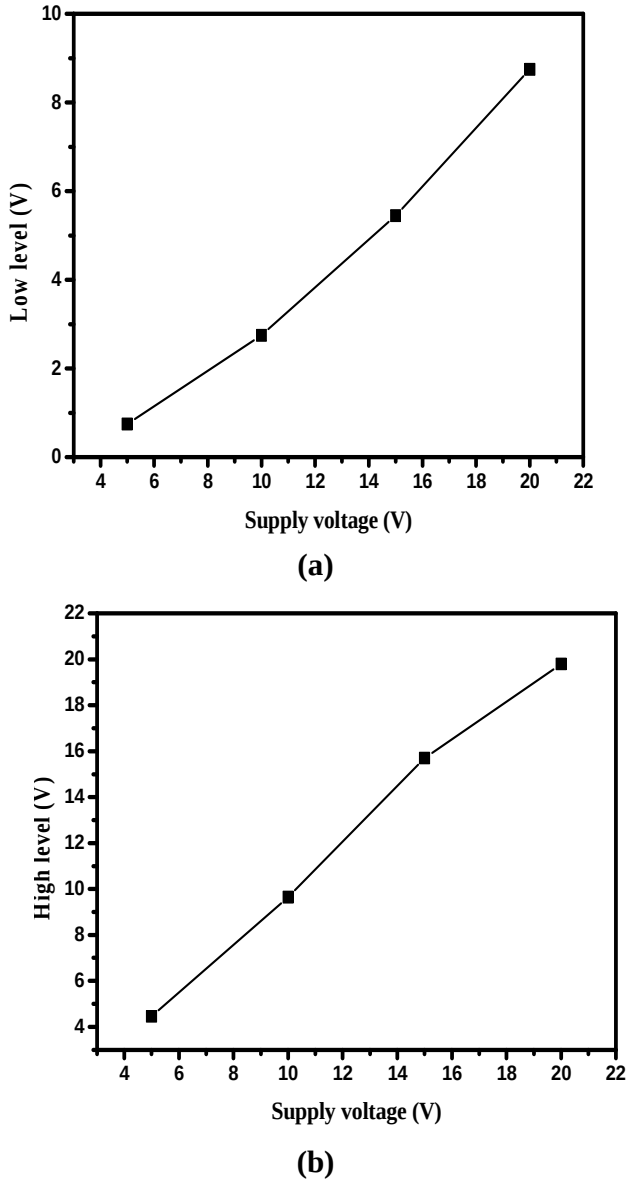


Figure 6. High (a) and Low (b) levels vs supply volage for a-Si NAND gate.

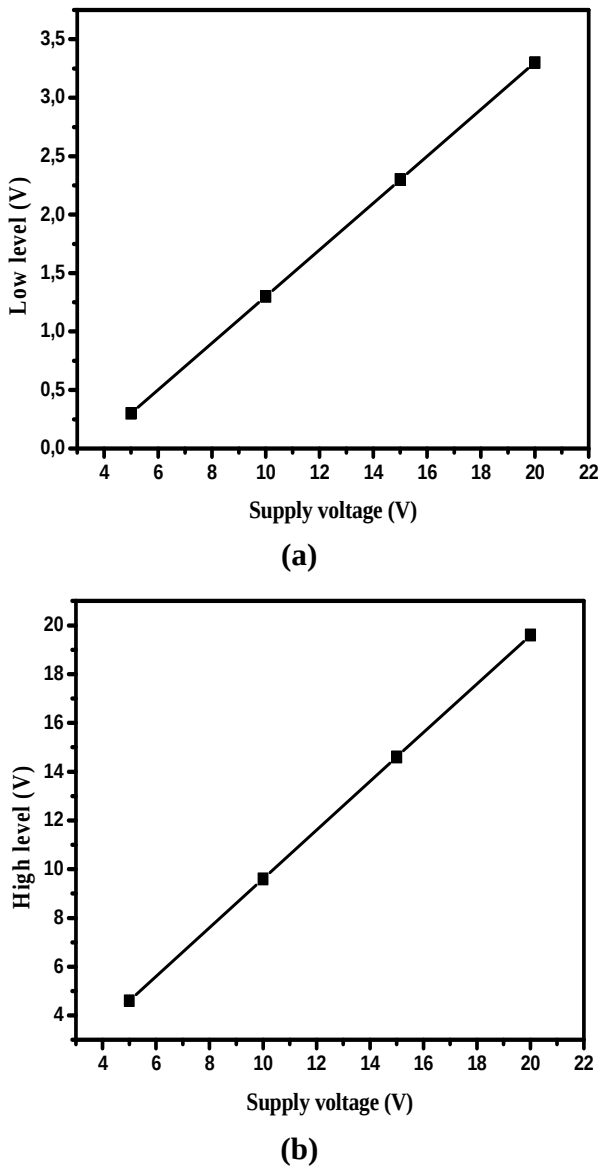


Figure 7. Low (a) and high (b) levels vs supply volage for a-Si NOR gate.

inputs is far from being negligible when the supply voltage is high which considerably degrades their performance.

Another important parameter which accounts for logic gates performance is the propagation delay. Figure 8 shows the evolution of this factor with supply voltage. Shorter propagation delays can be obtained when V_{dd} increases, revealing an increase in the charge careers energy whose mobility rises. Therefore to enhance the speed of the a-Si gates under study, V_{dd}, which determines the energy consumption, should be kept high.

The interest in the above gates is not only in defining their responses, but also in what they tell us about the effect of supply voltage on determining the gates' delays. Examination of simulation results enables us to make some useful observations which may illustrate the conflicting requirements and the trade-offs

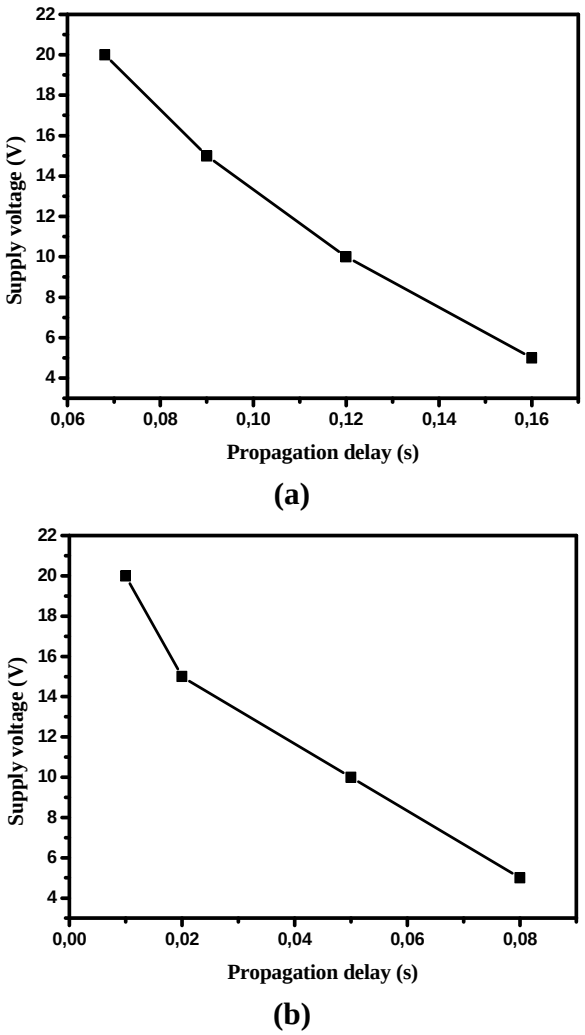


Figure 8. Propagation delay vs supply voltage for a-Si NAND (a) and a-Si NOR (b) gates.

available in the design of a-Si logic gates. Thus, in designing such gates, one should strive to reduce the supply voltage for noise immunity without affecting speed improvement.

4 CONCLUSION

Throughout this paper, the operation and characteristics of amorphous silicon based NAND and NOR gates circuits are thoroughly investigated. Earlier developed static and dynamic models for a-Si:H TFTs operations have been used to implement a model using LTspice. This may help integrated circuits design in amorphous silicon technology. The gates have been used to validate the model implementation and to take a more comprehensive look at these circuits, investigating their performance and exploring the trade-offs available in their design. The characterization included high and low logic levels and propagation delay revealing reliability in the implemented model. The results may serve as a foundation of the design of a-Si logic circuits and can be extended to more complex circuits.

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