Circuit Testing Method Based on Wavelets

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ABSTRACT

The paper presents the comparison of waveforms for the input stimulus of a circuit under test, using a testing system incorporated in an FPGA, relying on a method based on wavelet transformation of the supply current or load current waveforms. The method differentiates due to the incorporation of different signal inputs according to the needs of the tester and the specifications of the circuit. This is a distinctive and effective method that offers a single–point test measurement solution and may easily be adapted to test various other analog and mixed-signal systems. Experimental results, derived from measurement comparisons, are presented showing the effectiveness of the proposed testing scheme.

KEYWORDS

Wavelet, Testing System, FPGA, Fault Detection

1 INTRODUCTION

Fault detection and diagnosis as a core component of operations management automation techniques of fault detection, used on electronic component/devices, provides the manufacturers, worldwide, with the ability to enhance the good, reliable quality and operability of their respected products before shipping the products to their customers. In model-based fault detection techniques, a model of the system is used to decide about the occurrence of fault. The system model may be mathematical or knowledge based. The speeding up of the testing phase in components/devices, leads to increased productivity and the results preserves the reliability towards the operation of the produced electronic circuits and systems [1-6].
In recent years, supply current testing of analog circuits has been investigated and various approaches have emerged [7-10]. The determination of the "signature" which will be used in fault detection is crucial to the system. Among others, the root-mean-square (RMS) value of the supply current, the magnitude and phase components of its spectrum, (Fourier transform) have been used [11]. Another approach is based on the use of the wavelet transform, which resolves a signal in both time and frequency simultaneously [12-14]. It gives a better approximation of a transient current waveform than the Fourier transform for a certain frequency of the signal.

2 WAVELETS TRANSFORMATION AND TESTING METHOD

The wavelet transform [15-18] is a transform that provides both time and frequency representation. It passes the time-domain signal from high pass and low pass filters to filter out either high frequency or low frequency portions of the signal. This procedure is repeated, every time some portion of the signal, corresponding to some frequencies, is being removed from the signal. The procedure is called decomposition. The decomposition is repeated to a predefined decomposition level.
Next, a set of signals is produced which actually represents the original signal. For sampled signals (as in our case) the Discrete Wavelet Transform is used. The Haar transform [15-18] decomposes a discrete signal into two

subsignals of half its length. One subsignal is a running average or trend; the other subsignal is a running difference or fluctuation d.
Since the energy of the trend subsignal T accounts for a large percentage of the energy of the transformed signal, the energy is computed by considering only the trend coefficients of the first level decomposition as shown in Eq. 1:

$$E_T = \sum_{j=1}^{n} T_1^2 \quad (1)$$

The test method, which is effectively utilized by the test system, uses as a metric the energy value [15-18] of the wavelet transform of the measured power supply or load current waveforms. The test method is a two phase process. At the first phase (Initial Phase), the wavelet energy value of the reference circuit is measured and stored. In the second phase (Main Test Phase) the wavelet energy of the circuit under test (CUT) is measured and compared to the corresponding value of the reference circuit. The detection of a faulty circuit instance will be successful when its wavelet energy value exceeds certain tolerance limits. These limits are introduced in order to account for circuit parameter variations and measurement inaccuracies. Finally, the definitions of the wavelet energy for the reference circuit and the tolerance limits along with the percentage detectability values are calculated.

4 EXTERNAL TESTING SYSTEM

The external testing device measures the current signatures of power supply lines (I_{PS}) or load (I_L) of the CUT and classify the CUT accordingly. The tested current of the CUT is sampled by an external Analog to Digital Converter and is driven to the FPGA. The sampled data are led to the FPGA to be processed. The processed data provide the necessary information to create a signature database for comparing the "good" circuits against the measured CUTs for the good/fault classification. The comparison is initialized after the CUT's signature is extracted. Both signatures, the good one and the CUT's, are compared with the help of a distance metric. The comparison leads to a good/fault classification.

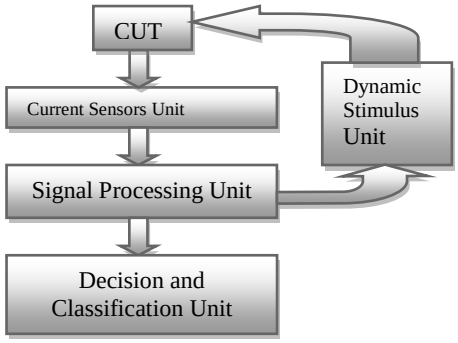

Figure 1 Procedural Block Diagram

The procedural block diagram of the system is illustrated in Figure 1.

4.1 FPGAs Signal Processing Unit

The sampled data from the A/D are led to the FPGA to be processed by a Digital Filter, embedded into the Signal Processing Unit which is located inside the FPGA and used for antiallising and denoising purposes [19].

4.2 FPGAs Dynamic Stimulus Unit

A novelty introduced is the Digital Stimulus Pattern Generator incorporated inside the FPGA. Its purpose is to apply the correct digital or analog signal (after a D/A conversion) to the CUT according to the specifications of the CUT. When a CUT cannot be classified from the signature taken for a specific stimulus, then the pattern generator creates a new stimulus that provides a new signature for comparison. This stimulus is created by LUT's, DDS and LFSR. The stimulus can also be user selectable, depending on the CUT.

4.3 FPGAs Decision and Classification Unit

All the digital processing, filtering, frequency component analysis, metric extraction and final good/faulty classification, is implemented

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inside the FPGA. The extracted energy of the signature, the RMS and mean values of the tested current signature are also calculated in the same unit. Finally, the calculated signature is compared to the data base signatures for comparing the "good" circuits against the measured CUTs for the good/fault classification. The software design is embedded into the Virtex-5LXT FPGA from Xilinx. The FPGA is finally populating onto the XUPV5-LX110T Development Board from Xilinx [20].

5 SOFTWARE REQUIRED

The selected software is Microsoft Windows 7 Professional 64bit Edition, Matlab 2011b incorporating Simulink 6.5 with the DSP 6.5 Toolbox and the Xilinx System Generator for DSP 13.2. Finally, the Xilinx ISE 13.2 edition is installed.

Three IP cores are used for the development of the system. The Xilinx FIR Compiler 5.0 and the Xilinx FFT 7.1 are part of the Xilinx System Generator for DSP Toolbox and an IP Core is developed incorporating the wavelet transformation for the extraction and calculation of the respective signature of the CUT.

The software portion of the system includes subroutines to control the peripheral devices of the FPGA in order to acquire data from the specific inputs, process them and display the results. The result is a reconfigurable testing system, able to support various circuits, in structural format.

The algorithm is as a sequence of steps where inputs and outputs take place. In every step, the voltage or current from the CUT is measured and processed according to the user requirements and specifications. The testing algorithm is saved in the EEPROM memory.

6 EXPERIMENTAL RESULTS

The system has been used for testing various well known mixed signal circuits and measurements have been taken from each one individually. Conclusions derived proving the functionality of the system. The measurements have been published in conferences around the world for each circuit [21] [22]. Based on the results of fault detectability from every circuit tested the following experimental results derived.

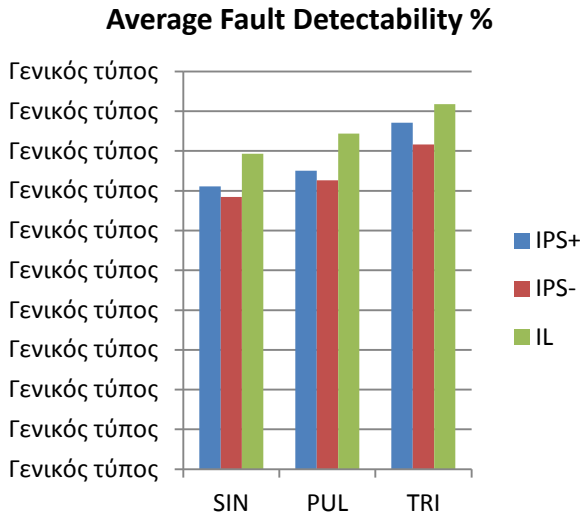

Figure 2 Average fault detectability

The graph of Figure 2 depicts the functionality of the system. The triangular input stimulus consistently outperforms the pulse input, while sinusoidal input signal follows with the lowest fault percentage detectability. The result is that the non-linear (pulse or triangular) input stimulus always gives larger fault detectability values than the linear sinusoidal signals. Moreover, the load current IL waveform always offers greater fault detection ability than the positive and negative current measurement waveforms.

7 CONCLUSIONS

The selection and comparison of the input stimulus using a testing system based on a method incorporating wavelet transformation of the supply current or load current waveforms using FPGAs is presented. An advantage of the method is its simplicity, the single measured signal (a single current) and the single test point. For the examined circuit cases, it is

observed that the utilization of the I_L current measurements by the proposed test method may result in higher fault coverage than the use of the I_{PS} current.

Comparative results from three different input stimulus, show that the non-linear (pulse or triangular) input stimulus always gives larger fault detectability values than the linear sinusoidal signals.

Work is under way to exploit other testing methods using the implemented FPGA-based testing system in order to improve detectability, as well as to apply the presented method for testing other complex mixed-signal circuits

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