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Power Efficient Gurumukhi Unicode Reader Design and Implementation on FPGA

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***Abstract*—Gurumukhi is found to be the most widely used language of Pakistan, and it is ranked 3rd in Canada, 7th in India and almost 4th most spoken language in U.K. This Unicode Reader is cost effective solution for learning as well as understanding the Punjabi language by the people across the globe .This reader helps the user to understand, whether written text is consonants, vowels or digits of Gurumukhi scripts. This paper can also be the solution to the various problems occurred in research of Punjabi natural language processing. Hardware is designed for Gurumukhi Unicode Reader (GUR) and is implemented on Virtex-6 FPGA on Xilinx software. This GUR design is tested on different frequencies by applying frequency scaling techniques .The reader is also observed on different IO Standards of two logic families i.e. on SSTL (Stub-Series Terminated Logic) and LVDCI (Low Voltage Digitally Controlled Impedance) logic families to make this design more energy efficient. It is concluded that using LVDCI_DV2_15 rather than SSTL18_II_DCI, the total power can be saved up to 51.22% with the device operating at a frequency of 1MHz.**

Keywords*— *Energy Efficient, Gurmukhi Scripts, Unicode Reader, Punjabi Language Reader, Natural Language Processing

I. INTRODUCTION

Even in the era of computer and telecommunication, constant development efforts are still being made in order to make the communication faster, easy, economical and less burdensome. But we are still away from the dream in which the ideas and the information can be freely exchanged despite of the language and script in which the data is written/spoken. Unicode is a one step ahead in making this dream true. Unicode is a universal character encoding standard. Unicode is designed in order to support characters from all languages around the world, unlike ASCII codes which are designed only to describe few basic English characters. So in order to make communication in Gurumukhi more easy and compatible, Power Efficient Unicode Reader has been designed in the following paper that consumes less power and less energy in order the meet the energy crisis being faced by the world .For the implementation of Gurmukhi Unicode reader, many other languages Unicoder Readers were also being [1-5]. In order to design a power efficient Gurumukhi, the power utilities of SSTL (Stub-Series Terminated Logic) [6] & LVDCI (Low Voltage Digitally Controlled Impedance) [7] logic families are compared at different IO (Input-Output) standards [8-10]. The power utility of the device can also check at other logic families such as HSTL, LVCMOS, Mobile DDR [11-13]. In conjunction with the change in the IO standards, the frequency of the FPGA device has also been scaled from lowest frequency of 1MHz to the highest frequency of 1 THz in order to see the effect of the frequency on the total power consumption of the device, this process of scaling is called as frequency scaling [14]. The frequency can be varied to more than 1THz and to less than 1MHz.In this way by applying the frequency scaling technique and changing the IO standards the least power consumed IO standard and frequency has been find out , thus making the device power efficient by operating it on such a particular frequency and IO standard. Voltage scaling [15], Capacitance scaling [16] and many other powers efficient techniques can also be applied to the devices in order to make devices more power efficient.

II. SCHEMATIC OF GURMUKHI UNICODE READER

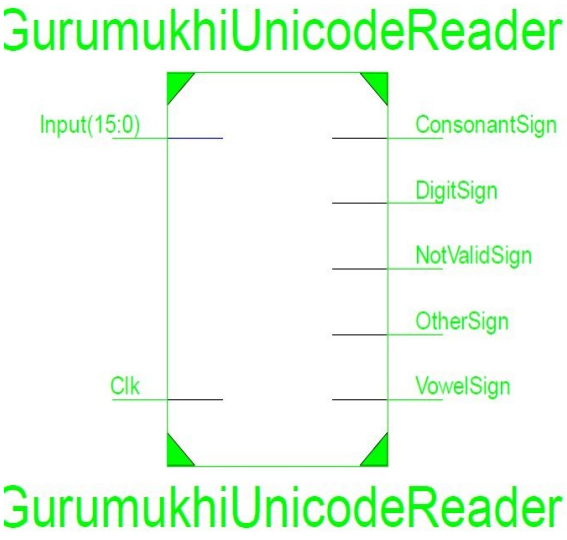

Fig. 1: RTL Schematic of Gurmukhi Unicode Reader

RTL (Register Transfer Level) schematic of the Gurumukhi Unicode reader is shown in the fig.1. Two inputs have been applied to the reader one is the 16 bit hexadecimal code which is unique for each and every alphabet or character of Gurumukhi. Another is the clock input in order to make it a synchronous circuit. Five corresponding outputs are coming out of the circuit. The hexadecimal range lies from 0x0A01-0x0A70 is solely dedicated to the characters of the Gurumukhi. If any range comes out to be less or more than this dedicated range, then not valid sign will be high, else if the hexadecimal input range confines within 0x0A05-0x0A14, then the output of the vowel sign will be high as shown in the figure 2. The input applied to the Gurmukhi Unicode Reader is 0x0A10 that lies within the ranges of Vowels of Gurmukhi language; hence the output is 1 corresponding to the vowel sign. Similarly if the input range lies within 0x0A15-0x0A39, then the output at the consonant sign will be high, if the input range lies within 0x0A66-0x0A6F, then the output at the digit sign will be high. If any other hexadecimal number is applied as an input within the range of 0x0A01-0x0A70 except the vowel, consonant and digit, then the output at other sign will be high.

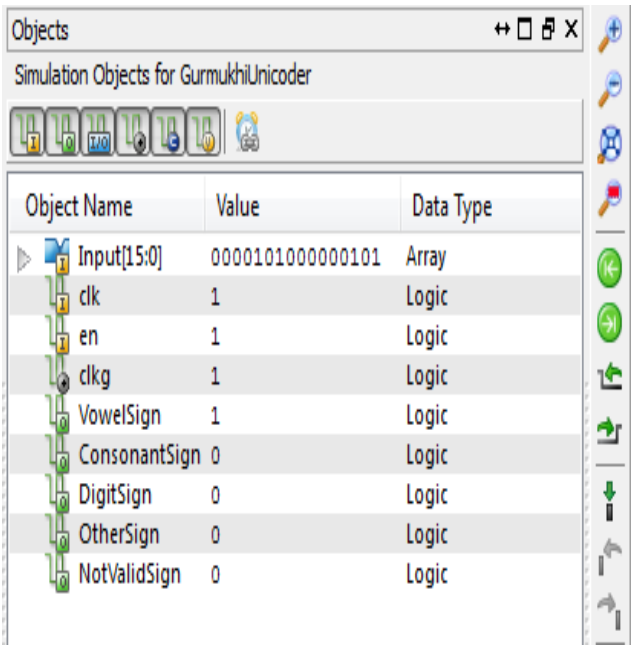

Fig. 2: Waveform of Gurmukhi Unicode Reader corresponding to the Vowel Sign

III RESULT ANALYSIS

The total amount of power dissipated by the device when operated at 6 different IO standards of SSTL and LVDCI logic family and 6 differe frequency ranges as depicted in the result analysis.

(i)Total power dissipated when the device operates at LVDCI_15, SSTL2_II IO standards and when its frequency is also scaled from 1 MHz to 1THz as shown in table 1.

Table 1: Power Analysis

Frequencies	Total Power Dissipated (LVDCI_15)	Total Power Dissipated (SSTL2_II)
I THz	32.325	39.921
100GHz	3.927	4.980
10GHz	1.040	1.417
1GHz	0.750	1.061
100MHz	0.721	1.024
10MHz	0.718	1.021
1MHz	0.718	1.020

It has been observed that out of all the frequencies the frequency at which the amount of dissipation of power minimum is a frequency of 1MHz whereas the maximum power is dissipated at highest 1THz frequency. It has also been observed that out of LVDCI_15 and SSTL2_II IO standards , SSTL2_II is the one at which the dissipation of power is maximum as compared to LVDCI_15.Hence it is most feasible to work with LVDCI logic family in comparison to SSTL. Mathematically there is 97.7% of power is reduced on operating at 1 MHz frequency rather than 1THz in case of LVDCI_15 and there is 97.4% reduction in power of SSTL2_II. Hence if we compare both LVDCI_15 and SSTL2_II families, then it can be concluded that on operating the device at a frequency of 1MHz in case of LVDCI_15, we can save total 29.6% of dissipated power rather than in case of SSTL2_II as shown in figure3.

Fig. 3: Comparison of Power Dissipation with LVDCI_15 and SSTL2_II

(ii)Total power dissipated when the device operates at LVDCI_18, SSTL18_II IO standards and when its frequency is also scaled from 1 MHz to 1THz as shown in table 2.

Table 2: Power Analysis

Frequencies	Total Power Dissipated (LVDCI_18)	Total Power Dissipated (SSTL18_II)
I THz	36.678	34.621
100GHz	4.378	4.426
10GHz	1.089	1.351
1GHz	0.760	1.044
100MHz	0.726	1.012
10MHz	0.723	1.009
1MHz	0.723	1.009

It has been observed that out of all the frequencies the frequency at which the amount of dissipation of power minimum is a frequency of 1MHz whereas the maximum power is dissipated at highest 1THz frequency. . It has also been observed that out of LVDCI_18 and SSTL18_II IO standards , SSTL18_II is the one at which the dissipation of power is maximum as compared to LVDCI_18.Hence it is most feasible to work with LVDCI logic family in comparison to SSTL. Mathematically there is 98.0% of power is reduced on operating at 1 MHz frequency rather than 1THz in case of LVDCI_18 and there is 97.08% reduction in power of SSTL18_II. Hence if we compare both LVDCI_18 and SSTL18_II families, then it can be concluded that on operating the device at a frequency of 1MHz in case of LVDCI_18, we can save total 28.34% of dissipated power rather than in case of SSTL18_II as shown in figure 4.

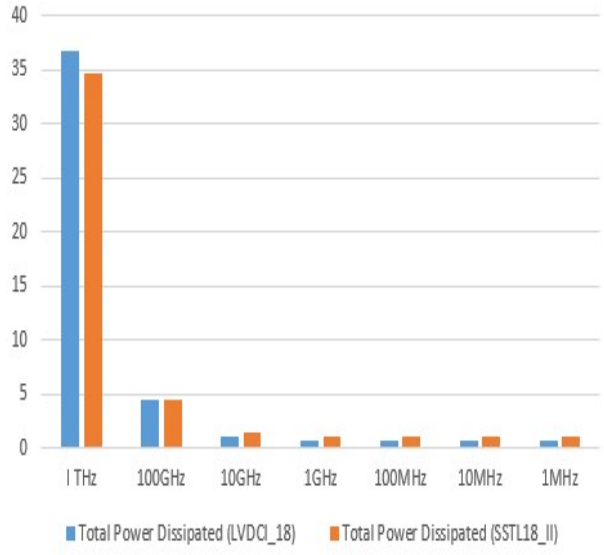

Fig. 4: Comparison of Power Dissipation between LVDCI_18 and SSTL18_II

(iii)Total power dissipated when the device operates at LVDCI_25, SSTL15 IO standards and when its frequency is also scaled from 1 MHz to 1THz as shown in table 3.

Table 3: Power Analysis

Frequencies	Total Power Dissipated (LVDCI_25)	Total Power Dissipated (SSTL15)
I THz	46.967	33.384
100GHz	5.450	4.827
10GHz	1.210	1.326
1GHz	0.786	1.030
100MHz	0.743	0.999
10MHz	0.739	0.996
1MHz	0.738	0.996

It has been observed that out of all the frequencies the frequency at which the amount of dissipation of power minimum is a frequency of 1MHz whereas the maximum power is dissipated at highest 1THz frequency. . It has also been observed that out of LVDCI_25 and SSTL15 IO standards , SSTL15 is the one at which the dissipation of power is maximum as compared to LVDCI_25.Hence it is most feasible to work with LVDCI logic family in comparison to SSTL. Mathematically there is 98.42% of power is reduced on operating at 1 MHz frequency rather than 1THz in case of LVDCI_25 and there is 97.01% reduction in power of SSTL15. Hence if we compare both LVDCI_25 and SSTL15 families, then it can be concluded that on operating the device at a frequency of 1MHz in case of LVDCI_25, we can save total 25.90% of dissipated power rather than in case of SSTL15 as shown in figure 5.

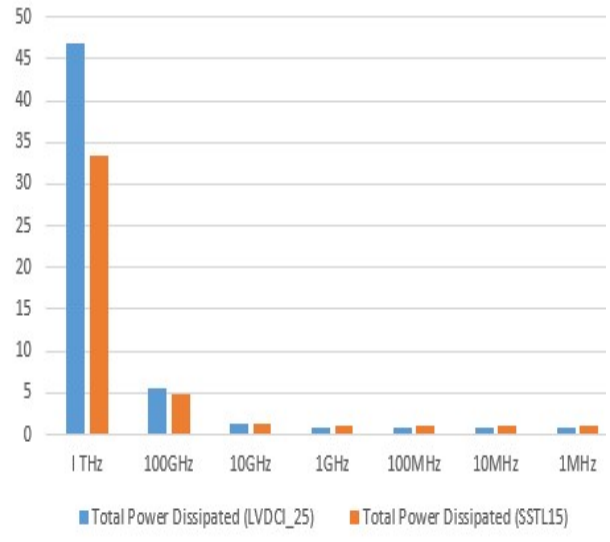

Fig. 5: Comparison of Power Dissipation between LVDCI_25 and SSTL15

(iv)Total power dissipated when the device operates at LVDCI_DV2_15, SSTL2_II_DCI IO standards and when its

frequency is also scaled from 1 MHz to 1THz as shown in table 4.

Table 4: Power Analysis

Frequencies	Total Power Dissipated (LVDCI_DV2_15)	Total Power Dissipated (SSTL2_II_DCI)
I THz	32.321	32.419
100GHz	3.923	5.075
10GHz	1.036	2.289
1GHz	0.747	2.011
100MHz	0.717	1.982
10MHz	0.714	1.979
1MHz	0.714	1.979

It has been observed that out of all the frequencies the frequency at which the amount of dissipation of power minimum is a frequency of 1MHz whereas the maximum power is dissipated at highest 1THz frequency. . It has also been observed that out of LVDCI_DV2_15 and SSTL2_II_DCI IO standards , SSTL2_II_DCI is the one at which the dissipation of power is maximum as compared to LVDCI_DV2_15.Hence it is most feasible to work with LVDCI logic family in comparison to SSTL. Mathematically there is 98.0% of power is reduced on operating at 1 MHz frequency rather than 1THz in case of LVDCI_DV2_15 and there is 97.08% reduction in power of SSTL2_II_DCI. Hence if we compare both LVDCI_DV2_15 and SSTL2_II_DCI families, then it can be concluded that on operating the device at a frequency of 1MHz in case of LVDCI_DV2_15, we can save total 28.34% of dissipated power rather than in case of SSTL2_II_DCI as shown in figure 6.

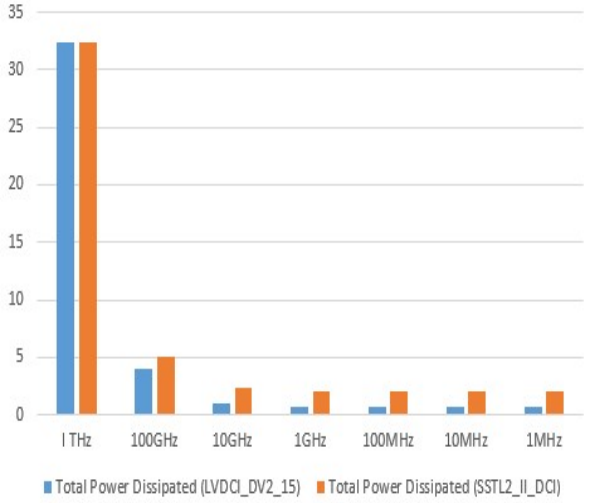

Fig. 6: Comparison of Power Dissipation between LVDCI_DV2_15 and SSTL2_II_DCI

(v)Total power dissipated when the device operates at LVDCI_DV2_18, SSTL18_II_DCI IO standards and when its frequency is also scaled from 1 MHz to 1THz as shown in table 5.

Table 5: Power Analysis

Frequencies	Total Power Dissipated (LVDCI_DV2_18)	Total Power Dissipated (SSTL18_II_DCI)
I THz	36.673	32.709
100GHz	4.373	4.645
10GHz	1.083	1.788
1GHz	0.754	1.502
100MHz	0.720	1.473
10MHz	0.717	1.470
1MHz	0.717	1.470

It has been observed that out of all the frequencies the frequency at which the amount of dissipation of power minimum is a frequency of 1MHz whereas the maximum power is dissipated at highest 1THz frequency. . It has also been observed that out of LVDCI_DV2_18 and SSTL18_II_DCI IO standards , SSTL18_II_DCI is the one at which the dissipation of power is maximum as compared to LVDCI_DV2_18.Hence it is most feasible to work with LVDCI logic family in comparison to SSTL. Mathematically there is 98.04% of power is reduced on operating at 1 MHz frequency rather than 1THz in case of LVDCI_DV2_18 and there is 95.50% reduction in power of SSTL18_II_DCI. Hence if we compare both LVDCI_DV2_18 and SSTL18_II_DCI families, then it can be concluded that on operating the device at a frequency of 1MHz in case of LVDCI_DV2_18, we can save total 51.22% of dissipated power rather than in case of SSTL18_II_DCI as shown in figure 7.

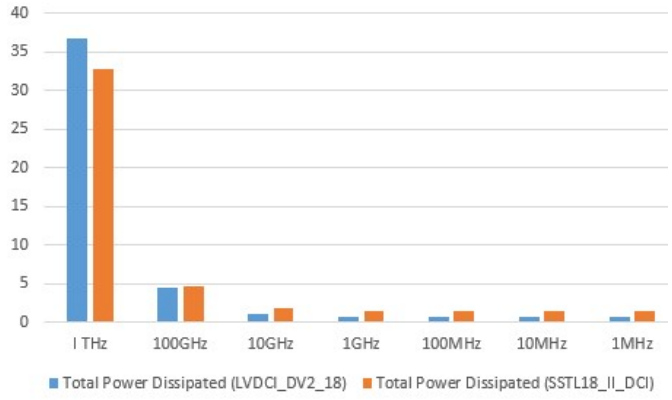

Fig. 7: Comparison of Power Dissipation between LVDCI_DV2_18 and SSTL18_II_DCI

(v)Total power dissipated when the device operates at LVDCI_DV2_25, SSTL15_II_DCI IO standards and when its frequency is also scaled from 1 MHz to 1THz as shown in table 6.

Table 6: Power Analysis

Frequencies	Total Power Dissipated (LVDCI_DV2_25)	Total Power Dissipated (SSTL15_DCI)
I THz	57.265	33.323
100GHz	6.497	4.499
10GHz	1.302	1.565
1GHz	0.783	1.271
100MHz	0.731	1.241
10MHz	0.725	1.238
1MHz	0.717	1.238

It has been observed that out of all the frequencies the frequency at which the amount of dissipation of power minimum is a frequency of 1MHz whereas the maximum power is dissipated at highest 1THz frequency. . It has also been observed that out of LVDCI_DV2_25 and SSTL15_DCI IO standards , SSTL15_DCI is the one at which the dissipation of power is maximum as compared to LVDCI_DV2_25.Hence it is most feasible to work with LVDCI logic family in comparison to SSTL. Mathematically there is 98.74% of power is reduced on operating at 1 MHz frequency rather than 1THz in case of LVDCI_DV2_25 and there is 96.28% reduction in power of SSTL15_DCI. Hence if we compare both LVDCI_DV2_25 and SSTL15_DCI families, then it can be concluded that on operating the device at a frequency of 1MHz in case of LVDCI_DV2_25, we can save total 42%of dissipated power rather than in case of SSTL15_DCI as shown in figure 8.

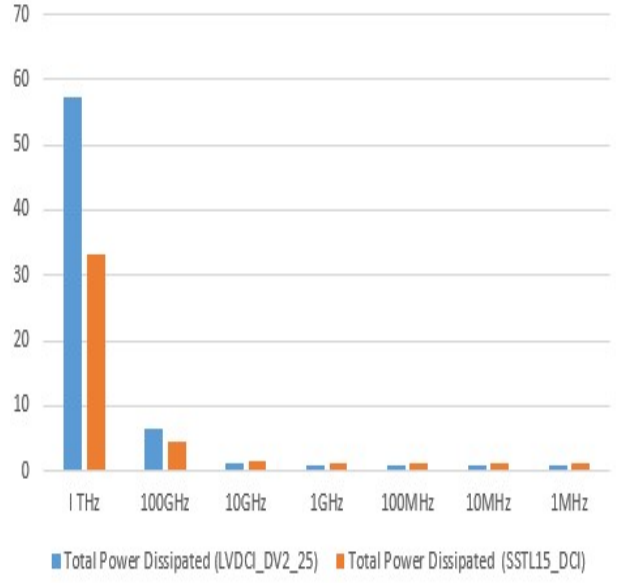

Fig. 8: Comparison of Power Dissipation between LVDCI_DV2_25 and SSTL15_DCIs

IV. Conclusion

It has been concluded that out of all the IO standards of SSTL and LVDCI logic families, the maximum amount of power has been saved in case of SSTL18_II_DCI if we want to operate the device on SSTL logic family and maximum power savage is in case of LVDCI_DV2_15 IO standard if we want to operate the device on LVDCI logic family providing that both the logic families are operating on a frequency of 1 MHz. Also if we compare amongst the two logic families, then it has been clearly seen from the table 7 that there is always a more power savage in case of LVDCI logic family in comparison to SSTL logic family.

Table 7: Comparison of Power Savage amongst LVDCI and SSTL logic family

S.NO.	If we move to	Power Saving
1.	LVDCI_DV2_15 rather than SSTL18_II_DCI	51.22%
2.	LVDCI_DV2_25 rather than SSTL15_DCI	42.08%
3.	LVDCI_15 rather than SSTL2_II	29.6%
4.	LVDCI_18 rather than SSTL18_II	28.34%
5.	LVDCI_DV2_15 rather than SSTL2_II_DCI.	28.34%
6.	LVDCI_25 rather than SSTL15	25.90%

It is concluded that the LVDCI_DV2_15 rather than SSTL18_II_DCI, the total power can be saved up to 51.22% with the device operating at a frequency of 1MHz.

V. Future Scope

We can also make the Unicoder on other languages such as Shahmukhi, Urdu, Sindhi and many more. Till now we have only worked upon the two logic families. We can also implement the same design on other logic families such as LCMOS, HSTL, LVPECL, RSDS and many more. In the implementation of Gurumukhi Unicode reader Virtex-6 FPGA has been used. There is further scope to implement the same design on some other advanced FPGA technologies such as Kintex-7 and Artix-7 in which the channel length of the gate is 28nm which is less than 40nm of Virtex-6.

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