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Low Noise Power Amplifier in 28-nm UTBB FDSOI Technology with Forward Body Bias

Ali Mohsen[1, 2], Adnan Harb[1], Senior, IEEE
[1]Department of Electrical and Electronics Engineering
Lebanese International University
146404 Mazraa, Beirut, Lebanon
Corresponding author: adnan.harb@liu.edu.lb

Nathalie Deltimple[2]
[2]IMS Laboratory
University of Bordeaux
351 Cours de la Libération
33405 Talence cedex
France

Abraham Serhane[3]
[3]Department of Industrial Engineering, Lebanese
Lebanese International University
146404 Mazraa, Beirut, Lebanon

***Abstract*—This paper presents a design of mm-wave LNPA which generates a large output power and low noise figure in one stage for a harmonic feedback oscillator block at the candidate of 5G; frequency 26 GHz. The LNPA is designed in the 28 nm UTBB FD-SOI. The benefits of this technology are stated with the effects of body biasing for the mm-wave LNPA. This amplifier is designed using a common source topology. It achieves 14 dBm P_{sat} and 2.5 dB noise figure "NF".**

Index Terms— LNPA: Low Noise Power Amplifies, UTBB FD-SOI: Ultra-Thin Body and Box Fully Depleted Silicon on Insulator, FBB: Forward Body Bias, NF: Noise Figure, PAE: Power Added Efficiency, P_{sat}: Saturated output power.

I. INTRODUCTION

A 28-nm FD-SOI (Fully Depleted Silicon On Insulator) transistor which is built without changing the fundamental geometry of the transistor lies on adding a thin insulator layer of buried oxide positioned under the channel as shown in Fig. 1. By that there is no need to add dopants to the channel due to the thin silicon film in the channel, thus making it fully depleted [1]. The net effect is that the gate can now control very tightly the full volume of the transistor body which makes it behave much better than a Bulk CMOS transistor. The technology of very thin buried oxide is called Ultra-Thin Body and Buried Oxide (UTBB). The buried oxide insulator layer confines the electron when flowing from the source to the drain [2] as shown in Fig. 2. So, it reduces the leakage current from the channel to the substrate.

Also, the absence of channel doping and pocket implants in the fully depleted transistor produces lower noise specifications and higher gains when compared to bulk technologies. To improve the transistor performance, a voltage can be applied to the substrate. This method is called 'Body Biasing' which facilitates the creation of the channel between the source and the drain resulting a faster switching. Because of the ultra-thin layer in FD-SOI, the biasing creates a buried gate below the channel making the transistor act as a double vertical gate transistor. This Ultra-Thin Body and BOX (UTBB) FD-SOI transistor architecture –7 nm silicon thickness and 25nm BOX thickness- has a stronger body effect than bulk transistors and therefore enables effective threshold voltage (V_{th}) management through body biasing. The 25 nm BOX thickness is a compromise between an increased parasitic source/drain to substrate capacitance and enhanced body effect. The range of back-gate biasing in UTBB FD-SOI is quite wider by a factor of 10 (i.e. -3V <VBB< 3 V) compared to the bulk technology (-300 mV <VBB< 300 mV). The low-V_{th} (LVT) transistors in the 28 nm UTBB FD-SOI CMOS process are fabricated as flip-well devices where the NMOS and PMOS devices are placed in the N-well and P-well respectively [3]. For the LVT transistors, the range of FBB voltages is [-0.3 V to +3 V] and [-3 V to +0.3 V] for the NMOS and PMOS respectively. Body bias can be used to vary the threshold voltage: while the FBB can be applied to decrease the threshold voltage, the RBB can be applied to increase it. It can be used to boost the performance by increasing the drive current and lowering the noise figure when applying FBB, and to decrease leakage. FBB also boosts the trans-conductance of MOS devices. Fig. 3 plots the g_m vs. V_{GS} of an LVT NMOS device with W/L = 2 µm/100 nm and V_{DD} = 1 V for different FBB voltages. At V_{GS} = 0.5 V, FBB = 3 V provides a g_m value which is 3.94 times that obtained at FBB = 0 V. Enhancement of g_m provides benefits such as increased unity-gain frequency, lower noise, etc. [4].

The total dielectric isolation of the channel in the UTBB FD-SOI creates lower gate and source/drain capacitance. And the raised-S/D (Source/Drain) epitaxy reduces the access resistance so the f_T/f_{MAX} will be increased; {f_T of N(P): 300(260) GHz and f_{MAX} of N(P): 170(120) GHz [5]}. Then the gain of the transistor will be increased too.

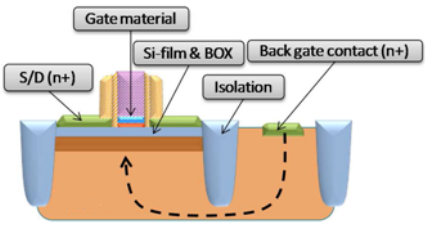

Fig. 1. UTBB FD-SOI Geometry

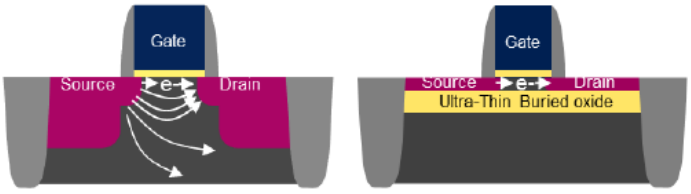

Fig. 2. Electron Flow

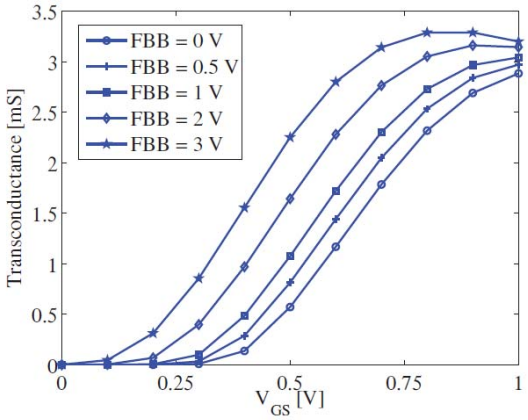

Fig. 3. Impact of FBB on Transconductance [4]

II. MM-WAVE LNPA DESIGN

Typically, a LNA is usually used in small signal circuits and is designed in the receiver block to amplify the detecting signal according to its sensitivity with low noise figure. Unlike a LNA, PA (Power amplifier) is used to amplify the large signal and mostly in the transmitter block; thus, the noise figure is not important in the PA. On the other hand, a LNPA, which this paper focuses on designing, is used to obtain a large output signal and low noise figure which can be used in harmonic feedback oscillator as shown in Fig. 4.b to ensure low phase noise.

The conventional feedback oscillator shown in Fig. 4.a is based on the Barkhausen criterion which states that the looped system starts oscillating at frequency F_0 so that between the input of the LNA and the output of the resonator it has a voltage gain higher than 0 dB and a phase shift multiple of 360 °.

A major concern about this type of structure is the disturbance of the output signal because of the variation of the output impedance (pulling /locking effect) and external current injections. Also, in terms of phase noise, performance - generally - can't meet the expected specifications for many applications. Such disadvantages have led to the development of phase-locked loop system (PLL) in the design of "Active RFID"; however, the use of phase locked loops reduces the total energy efficiency of the system and it increases - at the same time - the complexity of the circuit. Nevertheless, a PLL circuit leaves the door open to the effect of "pulling" that should be introduced in frequency and potential mitigation offsets.

To resolve those problems, a new architecture is proposed: Harmonic Feedback Oscillator. The idea is to replace the resonator structure by a diplexer port that will allow the feedback loop to ensure oscillation at the fundamental frequency F_0 being isolated from the output signal which is transmitted through the second harmonic $2F_0$ as shown in Fig. 4.b. This greatly reduces the impact of an output load variation of the feedback loop.

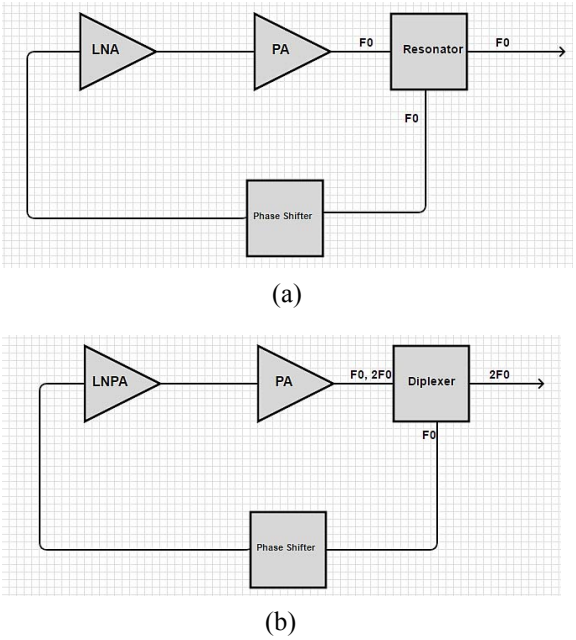

Fig. 4. Feedback Oscillator Diagram: (a): Conventional, (b): Harmonic

The common source (CS) and cascode topologies are used at millimeter frequencies._A transistor in common source has low power gain, problems with stability, and low output impedance. The C_{gd} capacity is like a feedback loop that degrades the insulation and gain. The C_{ds} capacity increases with the size increase of the transistor, and it consistently reduces the output impedance. This structure; nevertheless, achieves good voltage excursion which extends from the knee voltage to 2 V_{DD} in class A; thus, ensuring good linearity. The cascode structure that consists of two transistors has a priori better gain, better stability, and a wider bandwidth than the common source structure. Indeed, it reduces the input-output capacity and thus improves insulation. This circuit is much more sensitive to parasites, including those related to the connection between the two transistors. The C_{DSB} capacitance (source of the upper transistor, drain of the second transistor, and the body) formed with the substrate absorbs part of the millimeter signal and drops the gain. The output power is less than the common source and the noise figure is slightly bigger than of that in common source.

Table I. summarizes the performance of these two circuits, cascode and common source, according to the main characteristic parameters. We deduce the most suitable structure depending on the point to be optimized. Thus, a common source installation is recommended if you wish to allow the high output

power, low noise figure, good linearity, and efficiency. A cascode arrangement is more suitable for the realization of broadband circuits due to its high stability which facilitates impedance matching.

The single end LNPA amplifier of common source topology is designed to achieve low noise figure, and high output power in one stage. Then the circuit will have small area and low cost. The technology used is the 28 nm UTBB FD-SOI LVT_NFET from STMicroelectronics. The supply is 1 V and the frequency of operation is 26 GHz which is a candidate for a 5G band consideration. The LNA is designed with the forward body bias FBB to boost the performance of the gain and output power as well as the noise figure. As shown in Fig. 5, the drain current of the transistor which has grounded body bias is around 136 mA. While the FBB reaches 2V, the drain current increases to reach 183 mA. This leads to increase the gain as well the output power.

In the design process of the LNPA, there is a trade-off between the noise matching and the power. This problem can be resolved by adjusting the biasing of the transistor input to reduce the noise sensitivity parameter R_n, so that it reduces the dependence of noise figure, NF, on the noise match [6] as shown in (1).

$$F = F_{min} + R_n . R_s \left| Y_{opt} - Y_s \right|^2 \qquad (1)$$

Where F is the noise figure, Y_{opt} is the optimal source admittance for noise matching, and Y_s is the source admittance.

The DC bias is chosen to be 0.5 V to have the optimum noise figure as shown in Fig. 6. At this point, the LNPA will be in class A which is described with high gain and high linearity.

The LNPA circuit is shown in Fig. 7. The matching circuits used lumped elements of real model which belong to the 28nm FD-SOI kits. The output matching circuit is a trade-off between the optimum impedance for output power and optimum impedance for noise figure. C_1 and C_2 are DC blocks capacitors; and L_1 is RF choke of 1 nH. Transistor's width of 150 µm of 150 finger (1µm each) is chosen to handle the input power and to reduce the gate resistance R_g and hence R_n in (1).

The Fig. 8 shows the S-parameters of the LNPA which is based on harmonic balance SP; it includes the effects of input power. The linear gain S_{21} is around 15dB and the input and output matching are around 10dB and 9dB respectively.

The noise figure is around 2.5 dB at 26 GHz as shown in Fig. 9. The output power is 11.7 dBm with PAE= 32 % at the 1 dB compression point and 14 dBm at saturated power with PAE_{max}= 55 % as shown in Fig. 10.

The performances are summarized and compared against recently reported and measured mm-wave LNAs and PAs in Table II. The proposed LNPA achieves the lowest noise figure NF as low as 2.5 dB, gain of 15dB according to one stage, and P_{sat} of 14 dBm. The circuit is designed with real model of the 28 nm Kit component and does not include the post layout extraction, so that the NF will increase a little bit and the output power will decrease a little bit if the circuit layout is extracted and then fabricated.

TABLE I. PERFORMANCE OF CS VS CASCODE

Type	Gain	Linearity	Bandwidth	NF	Output Power
CS	-	+	-	+	+
Cascode	+	-	+	-	-

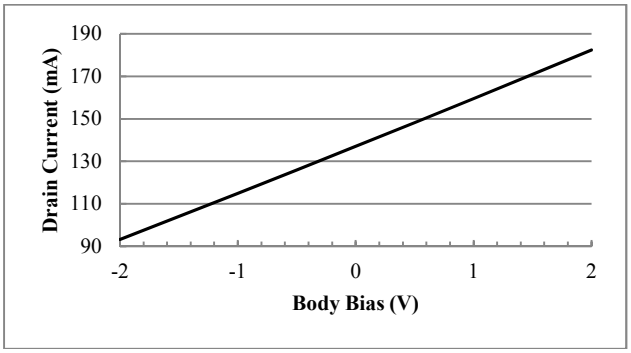

Fig. 5. Drain Current with Respect to Body Bias

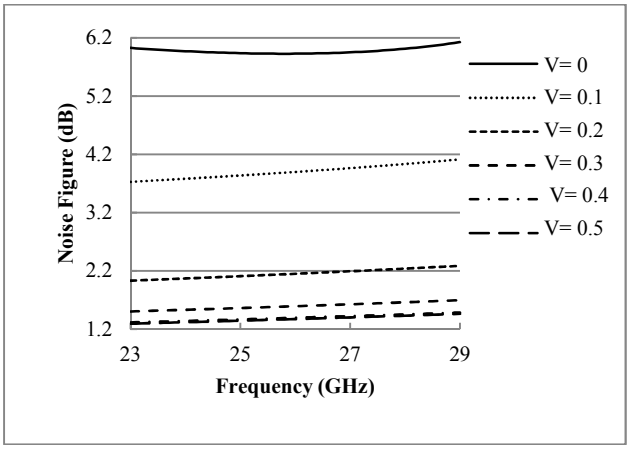

Fig. 6. Noise Figure at Different Biasing

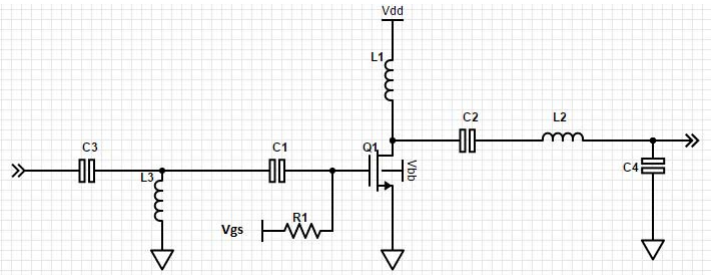

Fig. 7. LNPA Topology

TABLE II. LNAS AND PAS STATE OF ART

Reference/ Stage	CMOS Tech	Gain (dB)	NF (dB)	Center Freq.	P_{sat} (dBm)	PAE max %
[7]: LNA 1_stage CS	90 nm	13.8	3.8	37 G	--	--
[8]: PA 2_stages	65 nm	22	--	19 G	23.8	25.1
[9]: LNA 3_stages	65 nm	23	5.5	60 G	--	--
[10]: PA 1_stage	28 nm	10	--	28 G	14.8	36.5
[11]: LNA 3_stages	28 nm	23	4.5-5.8	50 G	--	--
This work: 1_stage	**28nm FDSOI**	**15**	**2.5**	**26 G**	**14**	**55**

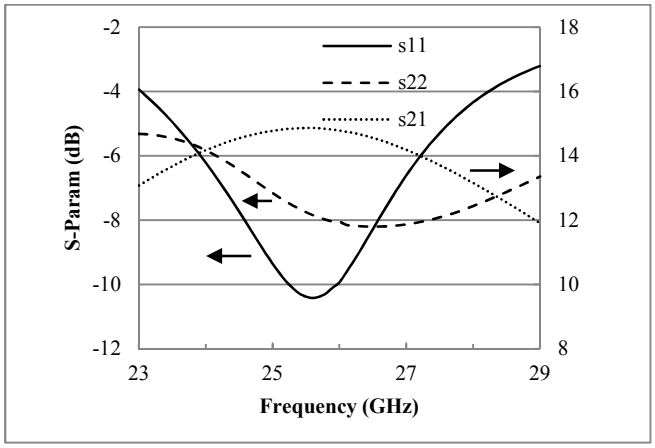

Fig. 8. LNPA S-Parameters

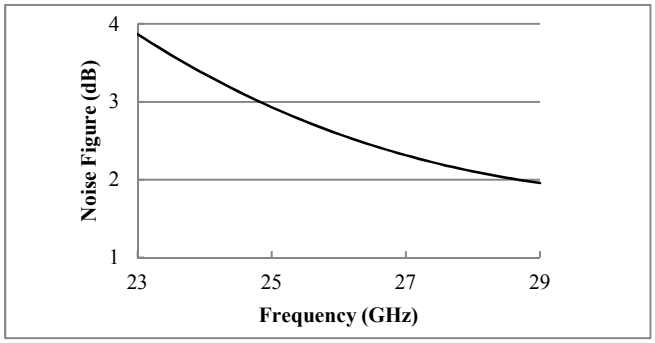

Fig. 9. Noise Figure

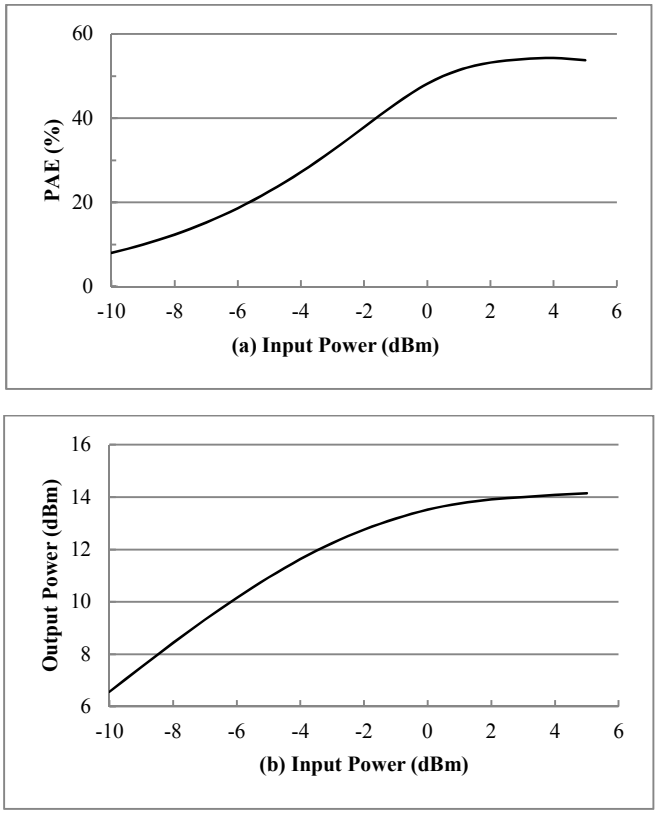

Fig. 10. Output Power and PAE vs. Input Power. (a) in percent and (b) in numerical values.

III. Conclusion

This paper provides an amplifier, LNPA, which joins between the low noise figure and high output power for a feedback oscillation block used in 5G application. The benefits of the technology UTBB FD-SOI used are explained, and the effects of the body bias technique are showed. Then the amplifier is designed to reach 2.5 dB noise figure and 14 dBm saturated power.

References

[1] P. Magarshack, P. Flatresse, and G. Cesana, "UTBB FD-SOI: a Process/Design symbiosis for breakthrough energy-efficiency," Design Automation & Test in Europe Conference & Exhibition (DATE), 2013, pp. 952 – 957.

[2] X. Federspiel, D. Angot, M. Rafik, F. Cacho, A. Bajolet, N. Planes, D. Roy, M. Haond, and F. Arnaud, "28nm node bulk vs FDSOI reliability comparison," IEEE Conf. Reliability Physics Symp. (IRPS), 2012.

[3] J. Lechevallier, R. Struiksma, H. Sherry, A. Cathelin, E. Klumperink, and B. Nauta, "5.5 A forward-body-bias tuned 450 MHz gm-c 3rd-order low-pass filter in 28nm utbb fd-SOI with >1dBvp iip3 over a 0.7-to-1 V supply," in ISSCC Dig. Tech. Papers, Feb. 2015, pp. 1–3.

[4] P. Harikumar, J. J. Wikner, and A. Alvandpour, "An ultra-low-voltage OTA in 28 nm UTBB FDSOI CMOS using forward body bias", 2015 Nordic Circuits and Systems Conference (NORCAS): NORCHIP & International Symposium on System-on-Chip (SoC), Year: 2015.

[5] A. Khakifirooz, K. Cheng, B. Jagannathan, P. Kulkarni, J. W. Sleight, D. Shahrjerdi, J. B. Chang, S. Lee, J. Li, H. Bu, R. Gauthier, B. Doris, and G. Shahidi, "Fully depleted extremely thin SOI for mainstream 20 nm low-power technology and beyond," IEEE International Solid-State Circuits Conference (ISSCC), pp. 152-153, 2010.

[6] A. Medra, V. Giannini, D. Guermandi, and P. Wambacq, "A 79-GHz variable gain low-noise amplifier and power amplifier in 28-nm CMOS operating up to 125 °C", European Solid State Circuits Conference (ESSCIRC), ESSCIRC 2014 - 40th.

[7] H. Yeh, C. Chiong, S. Aloui, and H. Wang, "Analysis and Design of Millimeter-Wave Low-Voltage CMOS Cascode LNA With Magnetic Coupled Technique," Microwave Theory and Techniques, IEEE Transactions on, vol. 60, no. 12, pp. 4066-4079, Dec. 2012.

[8] Y. Kawano, A. Mineyama, T. Suzuki, M. Sato, T. Hirose, and K. Joshin, "A fully-integrated K-band CMOS power amplifier with Psat of 23.8 dBm and PAE of 25.1 %," Proc. IEEE Radio Freq. Integr. Circuits Symp. Dig., pp. 5- 7, Jun. 2011.

[9] E. Cohen, O. Degani, D. Ritter, "A wideband gain-boosting 8 mW LNA with 23dB gain and 4dB NF in 65nm CMOS process for 60 GHz applications," Radio Frequency Integrated Circuits Symposium (RFIC), 2012 IEEE, pp. 207-210, June 2012.

[10] B. Park, D. Jeong, J. Kim, Y. Cho, K. Moon, and B. Kim, "Highly linear CMOS power amplifier for mm-wave applications", IEEE MTT-S International Microwave Symposium (IMS), 2016

[11] K. Hadipour, A. Ghilioni, A. Mazzanti, M. Bassi, and F. Svelto, "A 40 GHz to 67 GHz Bandwidth 23 dB Gain 5.8 dB Maximum NF mm-Wave LNA in 28nm CMOS", 2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Pages: 327 - 330, 2015.

